

MS7318M1 Version: 101

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CPU:

Intel LGA775

(Support Conroe E6300/E6400/E6700/E6800,
Prescott 500 Sequence, Cedar Mill,
Smithfield, Celeron D)

System Chipset:

VIA PT890CE (North Bridge)

VIA VT8251L (South Bridge)

On Board Chipset:

CLOCK - ICS953002 + ICS9P936

LPC Super I/O - W83627DHG

BIOS - LPC ROM

HD Audio ALC888

LAN - Realtek 8201CL colay RT8110SC

IEEE1394 - VT6308P

E-SATA JMB360

Main Memory:

single-channel - DDR2*2 533

Expansion Slots:

PCI Express X16 * 1

PCI 2.3 Slot * 1 (Medion 2 master)

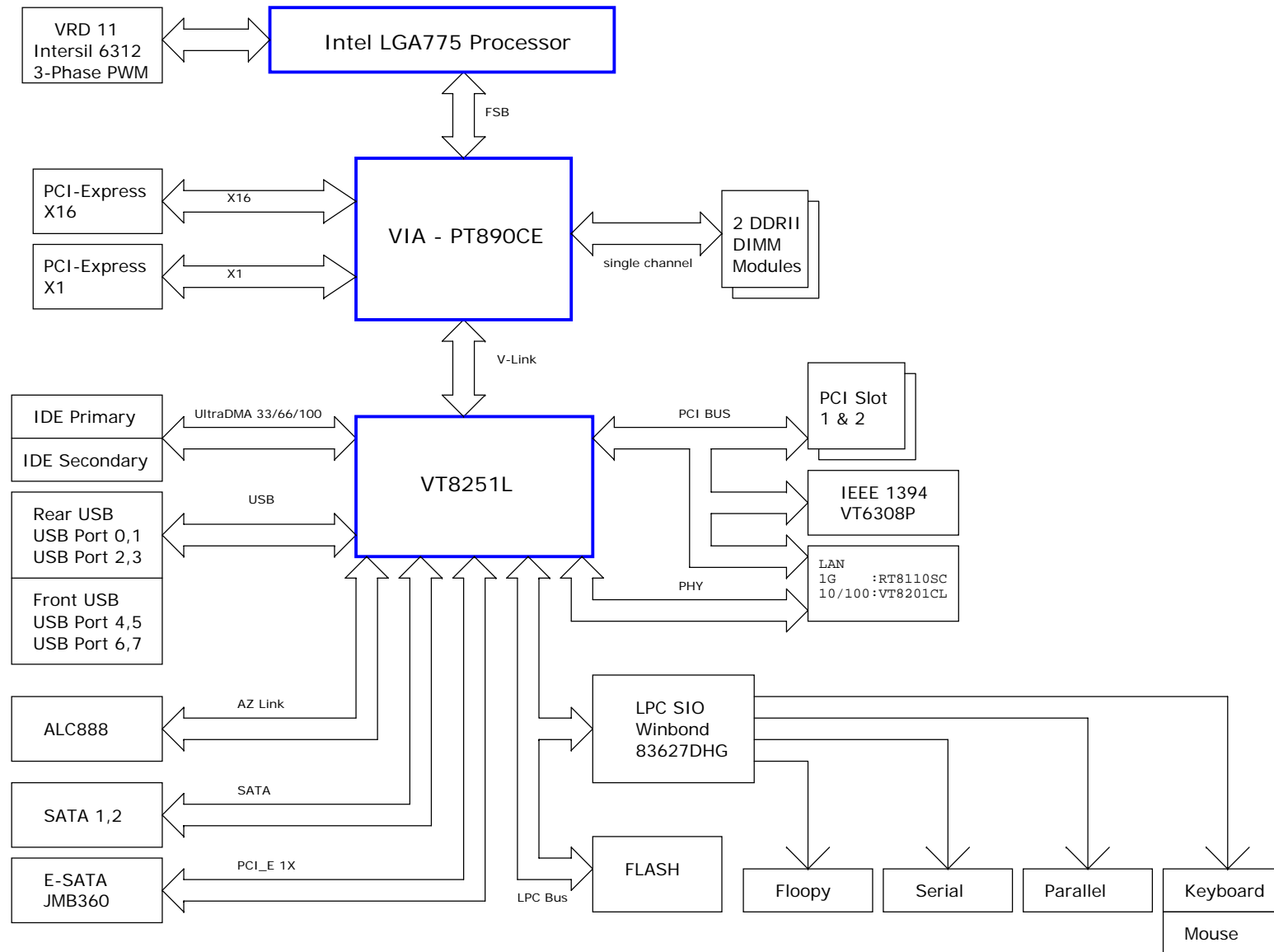
PCI 2.3 Slot * 1

PCI Express X1 * 1

PWM VRD11 :

Intersil 6312 3 Phase

Block Diagram



System Chipset General Purpose I/O					
Name	Pin	Type	Function Description	Normal	Activ
GP10	AB04	I	Pull High to VBAT	High	
GP11	AB02	I	Not Used; Pull High Only	High	
GP12/EXTSMI#	W02	I	EXTSMI#(Medion Funtion)	High	Low
GP13/RING#	Y03	I	RING#	High	Low
GP14/LID#	AA02	I	HM_SMI#	High	Low
GP15/BATLOW#	V01	I	Not Used; Pull High Only	High	
GP16/AGPBZ#	AF06	I	AGPBZ#		
GP17/REQ5#	L01	I	Not Used; Pull High Only	High	
GP19	A28	I	No Used; Pull Low Only	High	
GP116/REQ6#	M01	I	Not Used; Pull High Only	High	
GP117/CPUMISS/SACSDIN	U04	I	ATADET0; Low 80 pin cable		
GP118/THRM# / AOLGPI	W03	I	PEPMESCI#	VSUS33	
GP119/APICCLK	AB26	I	APICCLK		
GP120/ACSDIN2/PCS0#	T03	I	ACSDIN2		
GP121/ACSDIN3/PCS1#	T01	I	ACSDIN3		
GP122/SAGP1	AE08	I	Not Used; NC		
GP123/SAGP2	AF07	I	Not Used; NC		
GP128/SAGP3	AG07	I	Not Used; NC		
GP129/SAGP4	AF08	I	Not Used; NC		
GP132/INTE#	P04	I	Not Used; Pull High Only	High	
GP133/INTF#	N04	I	Not Used; Pull High Only	High	
GP134/INTG#	N01	I	Not Used; Pull High Only	High	
GP135/INTH#	N02	I	INTH#		
GP136/USB0C4#	B25	I	USB0C4#	High	Low
GP137/USB0C5#	A25	I	USB0C5#	High	Low
GP138/USB0C6#	A26	I	USB0C6#	High	Low
GP139/USB0C7#	D25	I	USB0C7#	High	Low
GP00	W04	O	EN_PCIERST	VSUS33	
GP01	AC01	O	Not Used; Pull High Only	High	
GP02/SUSA#	W01	O	Not Used; Pull High Only	High	
GP03/SUSST#	Y02	O	SUSST#	High	Low
GP04/SUSCLK	Y01	O	SUSCLK		
GP05/CPUSTP#	AD05	O	Not Used; Pull High Only	High	
GP06/PCISTP#	AD04	O	Not Used; Pull High Only	High	
GP07/GNT5#	M04	O	GNT5#		
GP08/GPI8/VGATE	AG06	O	Not Used; Pull High Only	High	
GP09	C27	O	Not Used; Pull Low Only		
GP020/GNT6#	N03	OD	GNT6#		
GP021/ACSDOUT1/SACSD	T02	OD	ACSDOUT1	VCC33	
GP022/GHI#	W28	OD	Not Used; Pull High Only	High	
GP023/DPSLP#	Y28	OD	Not Used; Pull High Only	High	
GP028/VIDSEL	AH06	OD	Not Used; Pull High Only	High	
GP029/VRDSLP	AE07	OD	Not Used; Pull High Only	High	
GP110/GP010/APICD0	W25	IO	Not Used; Pull High Only	VCC33	
GP1011/APICD1	W26	IO	Not Used; Pull High Only	VCC33	
GP1012/GPI0E/SACRST#	AH02	IO	Not Used; NC	VSUS33	
GP1013/GPI0F/SACBITCL	AG03	IO	Not Used; NC	VSUS33	
GP1014/GPI0G/SACYNC	AH03	IO	Not Used; NC	VSUS33	
GP1015/GPI0H	AF04	IO	Not Used; NC	VSUS33	
GP1024/GPI0A/PCREQA	AE03	IO	Not Used; Pull High Only	VCC33	
GP1025/GPI0B/PCREQB	AE01	IO	Not Used; Pull Low Only	VCC33	
GP1026/SMBDT2	AB03	IO	SMBDT2	VSUS33	
GP1027/SMBCK2	Y04	IO	SMBCK2	VSUS33	
GP1030/GPI0C/PCGNTA	AF03	IO	Not Used; Pull High Only	VCC33	
GP1031/GPI0D/PCGNTB	AC05	IO	Not Used; Pull Low Only	VCC33	

Super I/O General Purpose I/O Super I/O default clock frequency is 48MHz					
Name	Pin	Function Description	Normal	Activ	
GP10 / GPSA1	128	N/A			
GP11 / GPSB1	127	N/A			
GP12 / GPX1	126	N/A			
GP13 / GPX2	125	N/A			
GP14 / GPY2	124	N/A			
GP15 / GPY1	123	N/A			
GP16 / GPSB2	122	N/A			
GP17 / GPSA2	121	N/A			
GP20 / CPUFANOUT1	120	NC			
GP21 / CPUFANIN1	119	NC			
GP22 / SCE#	19	NC			
GP23 / SCK	2	33MHz clock output for Debug			
GP24 / MDAT#	66	MSDAT#			
GP25 / MCLK#	65	MSCLK#			
GP26 / KDAT#	63	KBDAT#			
GP27 / KCLK#	62	KB CLK#			
GP30	92	NC			
GP31	91	CPU_FAN_TYPE			
GP32 / PSTOUT2#	90	NC			
GP33 / PSTOUT3#	89	NC			
GP34 / RSTOUT4#	88	NC			
GP35	87	NC			
GP36	69	NC			
GP37	64	NC			
GP40 / RIB#	85	RIB#			
GP41 / DCDB#	84	DCDB#			
GP42 / IRTX / SOUTB	83	SOUTB_IRTX			
GP43 / IRRX / SINB	82	SINB_IRRX			
GP44 / DTRB#	81	DTRB#			
GP45 / RTSB#	80	DTSB#			
GP46 / DSRB#	79	DSRB#			
GP47 / CTSB#	78	CTSB#			
GP50 / EN_GTL / WDT0#	77	EN_GTL			
GP51 / RSMRST#	75	NC			
GP52 / SUSB#	73	SLP_S3#			
GP53 / PS0N#	72	PS_0N#(5vSB)			
GP54 / POROK	71	PWROK			
GP55 / SUSLED	70	NC			
GP56 / PSIN	68	PS_IN#			
GP57 / PSOUT	67	PWRBTN#			
GP60 / RIA#	57	RIA#			
GP61 / DCDA#	56	DCDA#			
GP62 / PENKBC / SOUTA	54	SOUTA			
GP63 / SINA	53	SINA			
GP64 / PENROM / DTRA#	52	DTRA#			
GP65 / HEFRAS / RTSA#	51	RTSA#			
GP66 / DSRA#	50	DSRA#			
GP67 / CTSA#	49	CTSA#			

PCI Config.

DEVICE	MCP1	INT Pin	REQ# / GNT#	IDSEL	CLOCK	CLK GEN Pin Out
PCI Slot 1	PIRQ#A					
	PIRQ#B PIRQ#C PIRQ#D		PREQ#0 PGNT#0	AD20	CK_PCI_CLK0	11
PCI Slot 2	PIRQ#B					
	PIRQ#C PIRQ#D PIRQ#A		PREQ#1 PGNT#1	AD21	CK_PCI_CLK1	14
PCI Slot 2	PIRQ#C					
	PIRQ#D PIRQ#A PIRQ#B		PREQ#2 PGNT#2	AD22	CK_PCI_CLK2	17
1394	PIRQ#D		PREQ#3 PGNT#3	AD23	1394_PCLK	13
LAN	PIRQ#A		PREQ#4 PGNT#4	AD24	PCI_CLK_LAN	13


PIRQ#A also link to NB PIN H13
PIRQ#H also link to NB PIN B6

PCI RESET DEVICE

Signals	Source	Target
PCIRST#	VT8237A	MS7
PCIRST#1	MS7	1394 & SPIO & BIOS
PCIRST#2	MS7	PCI slot 1-2
NB_RST#	MS7	NB_RST#
HDRST#	MS7	Primary, Scondary IDE
Rsmrst#	MS7	VT8237A
PCIE_Reset#	VT8237A	PCIE 1-2

DDR DIMM Config.

RAMTYPE	2 DDR DIMM
DIMM 1 Slave	1010 0000 (A0)
DIMM 2 Slave	1010 0010 (A2)

**MICRO-START INT'L CO.,LTD.**

Title

GPIO/Memory/PCI/HW Config.

Size

Document Number

MS-7318-101-060918A

Rev

100

Date

Monday, September 18, 2006

Sheet

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of

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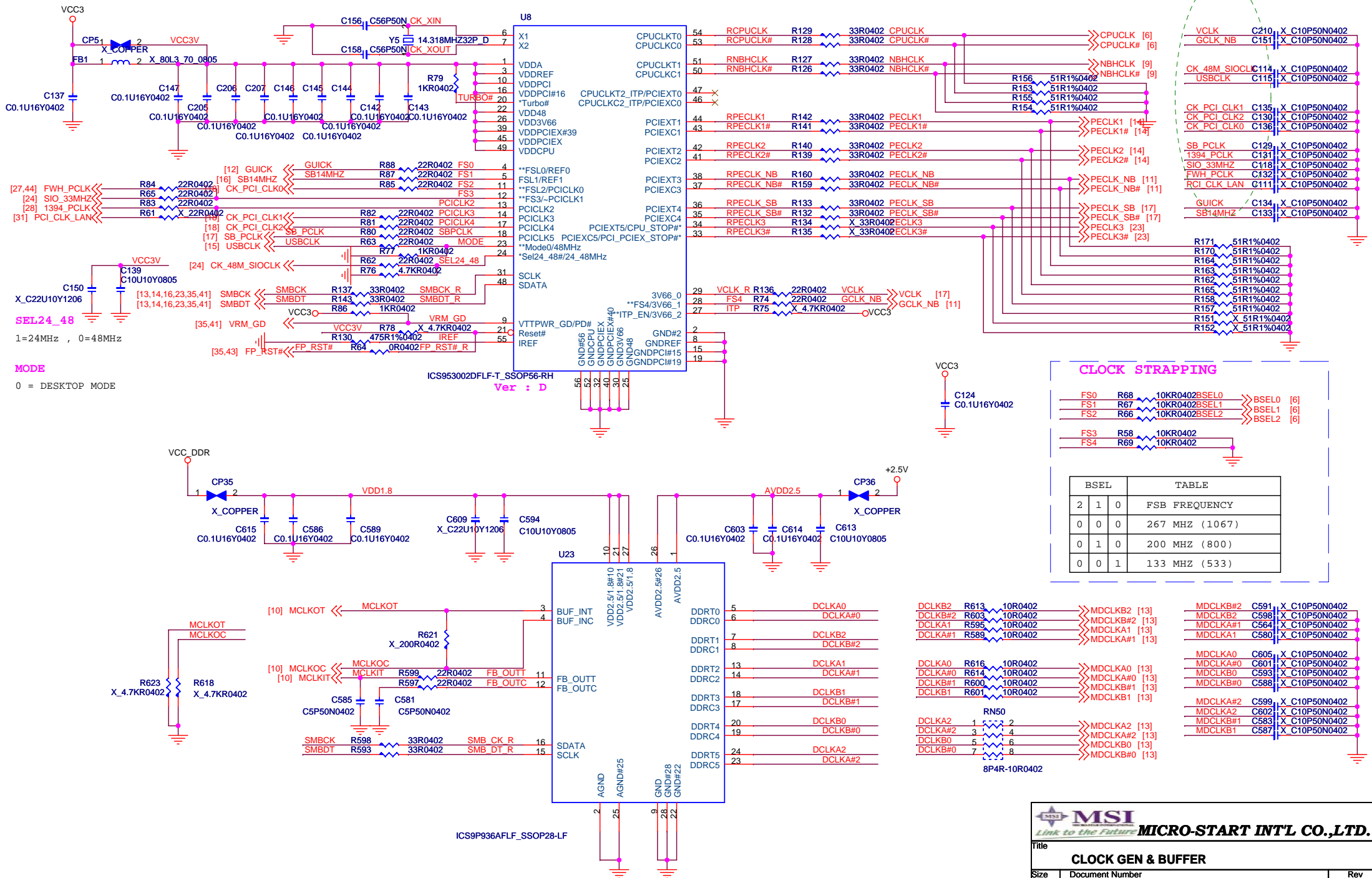
SB-VT5251LCE

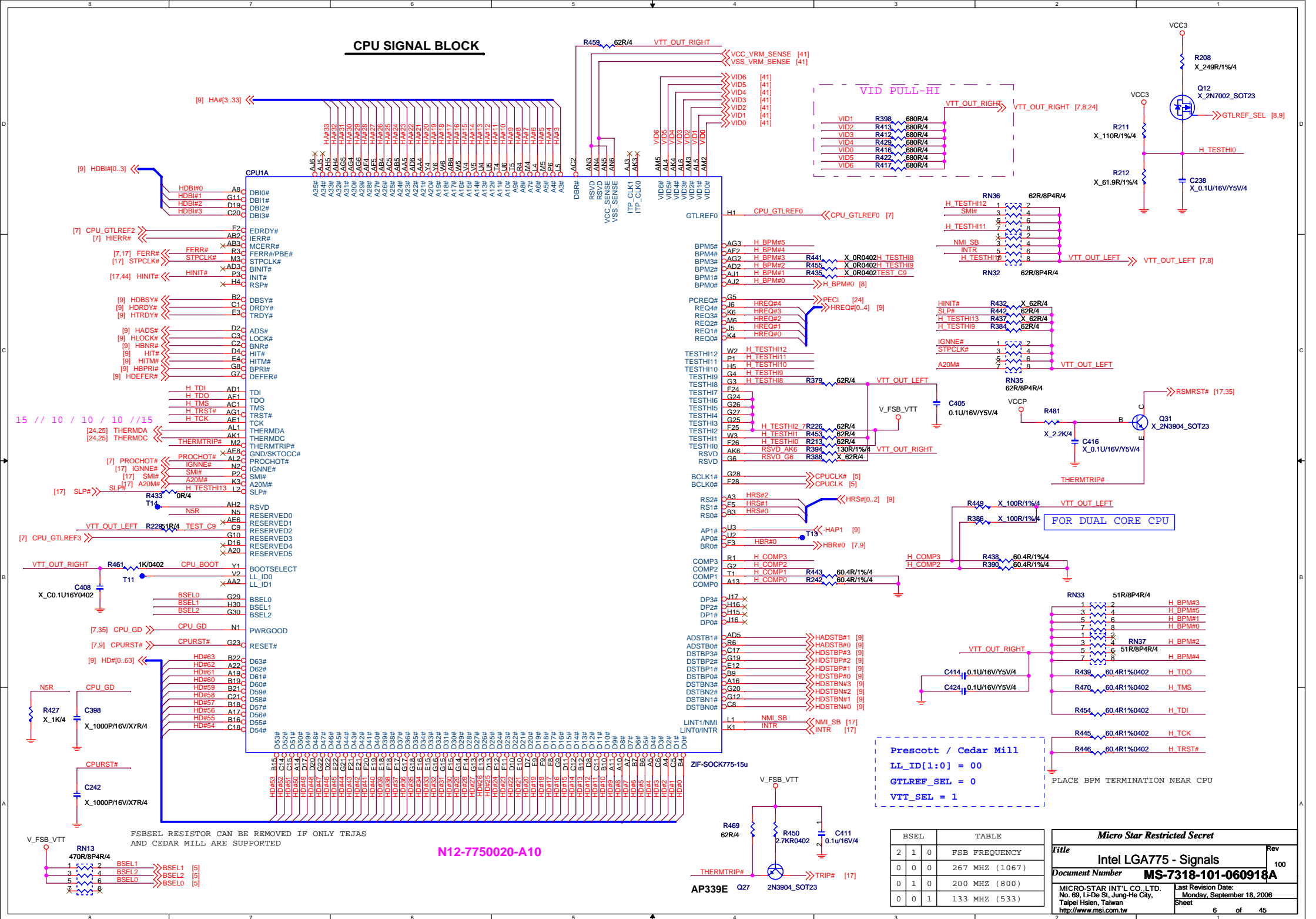
Strap Pins			
(External pullup / pulldown straps are required to select "H" / "L")			
Strap Pins for VT8251L Version CE Configuration			
Signal	Pin#	Function	Description
SPKR	AF05	CPU Frequency Strapping	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping Default setting: Disable
ACSDOUT0	R01	Auto Reboot	L: Enable Auto Reboot H: Disable Auto Reboot Default setting: Disable
SEEDI	B13	Use Serial External LAN EEPROM	L: Enable. Use external EEPROM H: Disable. Do not use external EEPROM Default setting: Enable (pull low) sInc
ACSYNC	R04	LPC FWH	L: Enable LPC FWH Command H: Disable LPC FWH Command Default setting: Disable
PDCS1#	AC25	SATA Spin Up Mode Vlink auto compensation	L: Enable SATA spin up mode iel H: Disable SATA spin up mode Default setting: Disable
PDDACK#	AB23	PCI Express Debugging Mode	L: Enable PCI Express debugging mode logntiaired H: Disable PCI Express debugging mode Default setting: Disable
SUSA#	W01	Notebook / Desktop LAN Reset	L: Notebook LAN reset H: Desktop LAN reset hnoideegu
Strap Pins for North Bridge ("NB") Configuration			
PDCS3#	AA23	NB Configuration ATeCon	PDCS3# signal state is reflected on signal pin VD7 during power up for North Bridge configuration.
PDA2	AD27	NB Configuration	PDA2 signal state is reflected on signal pin VD6 during power up for North Bridge configuration.
PDA1	AC26	NB Configuration	PDA1 signal state is reflected on signal pin VD5 during power up for North Bridge configuration. DAR
GPIOD / PCGNTB	AC05	NB Configuration	NGPIOD/PCGNTB signal state is reflected on signal pin VD3 during power up for North Bridge configuration.
GPIOB / PCREQB	AE01	NB Configuration	GPIOB/PCREQB signal state is reflected on signal pin VD2 during power up for North Bridge configuration.
PDA0, GPIOA/PCREQA, GPIOC/PCGNTA	AE03, AF03	NB Configuration	PDA0, GPIOA/PCREQA and GPIOC/PCGNTA signal states are reflected on signal pins VD4, VD1 and VD0 during power up for North Bridge configuration.

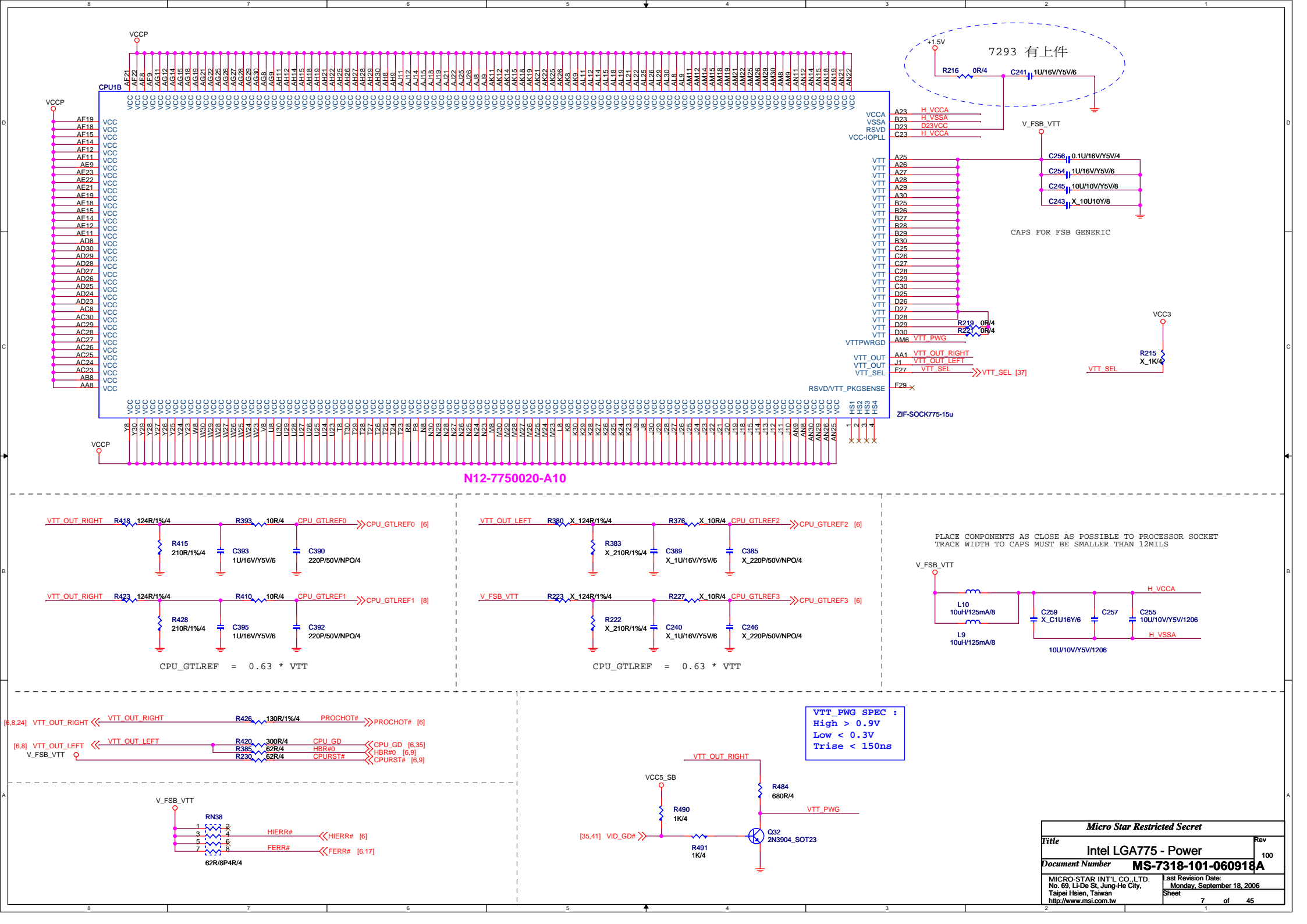
$$C_e = 2 \text{ CL} - C_i - C_s$$

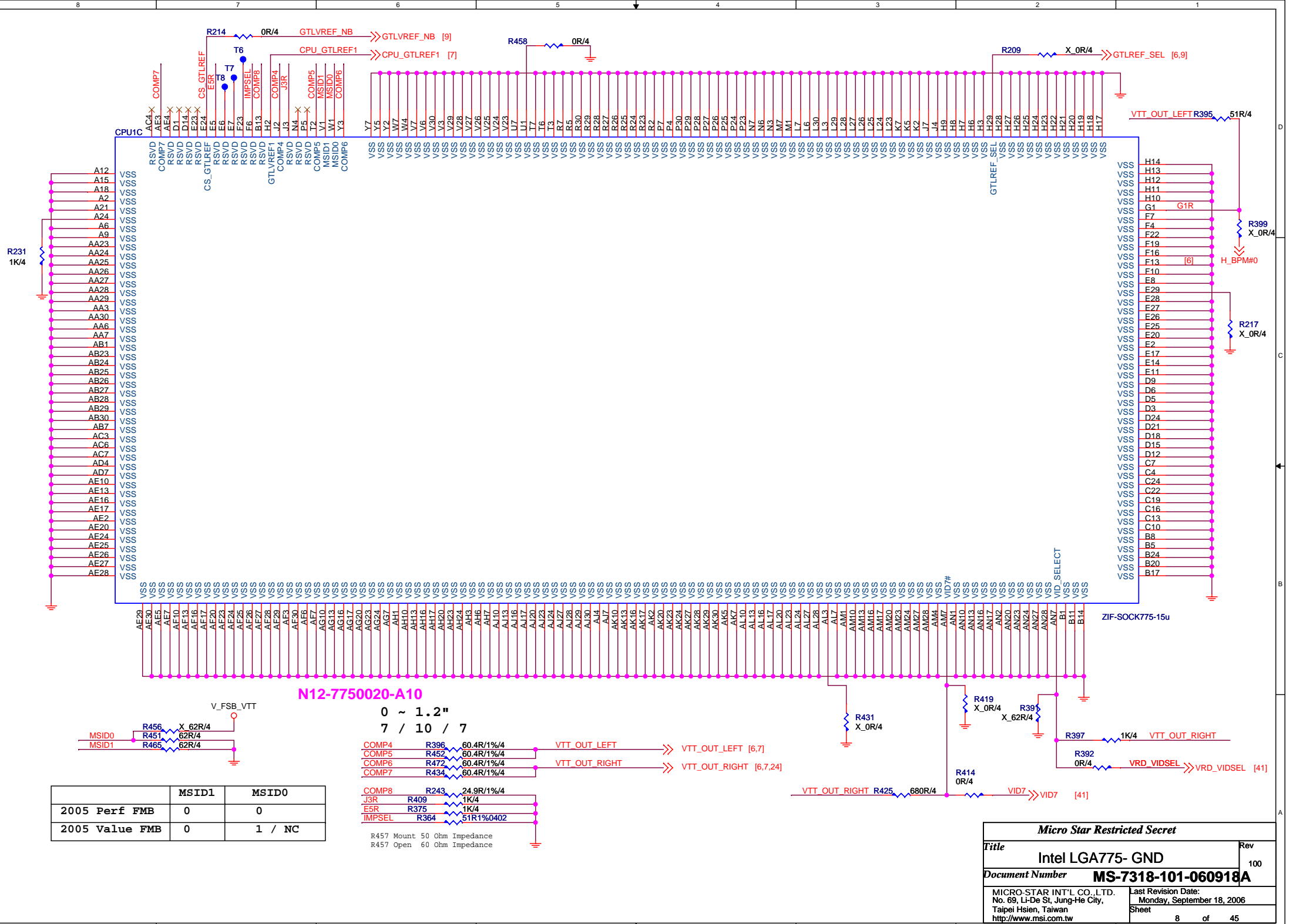
$$= (2 \times 32) - 5 - 3$$

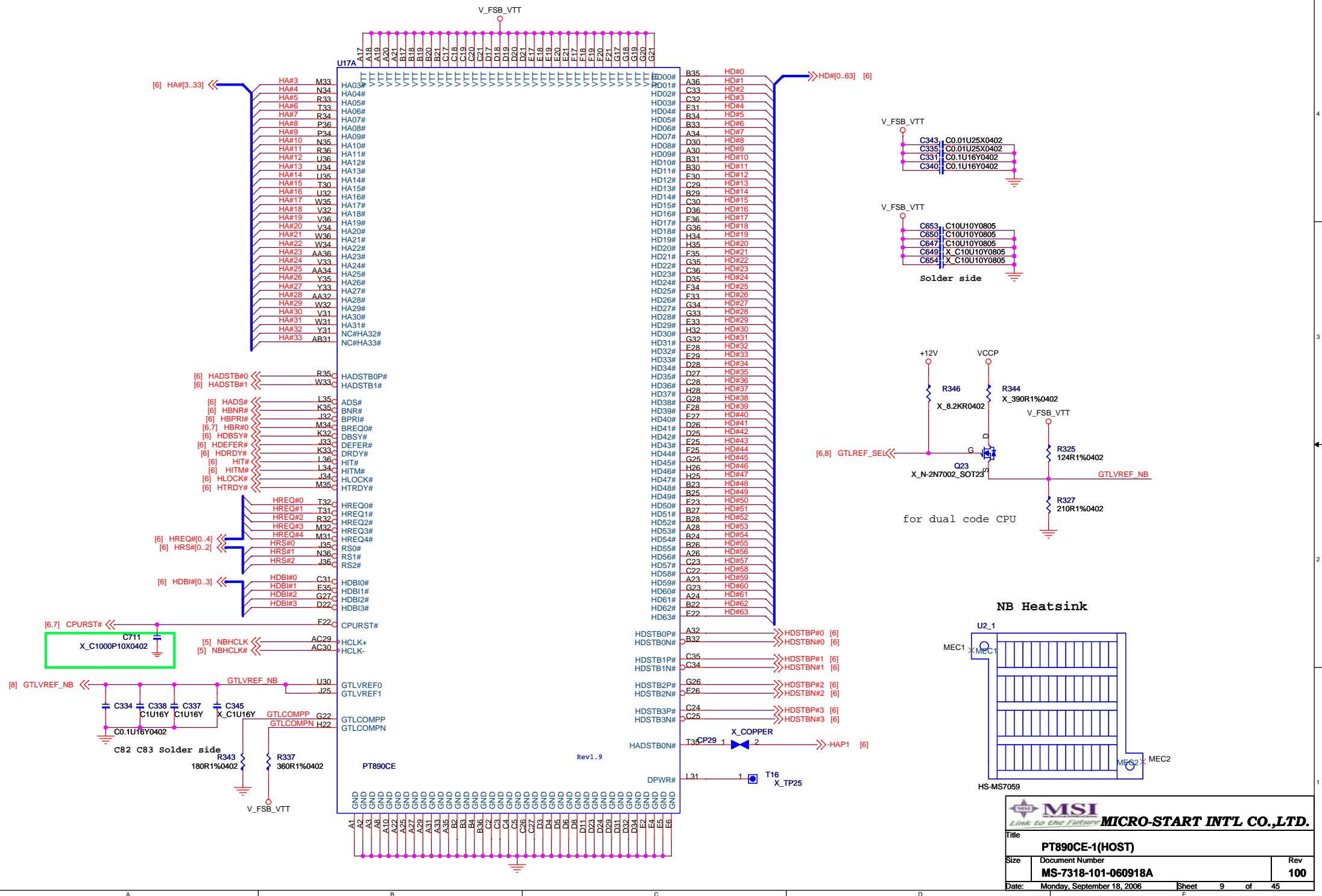
$$= 56$$





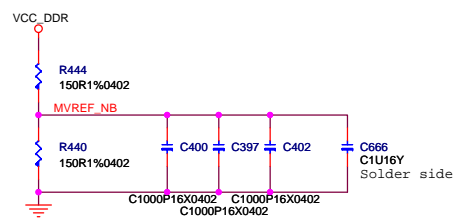
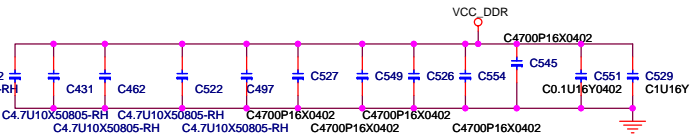
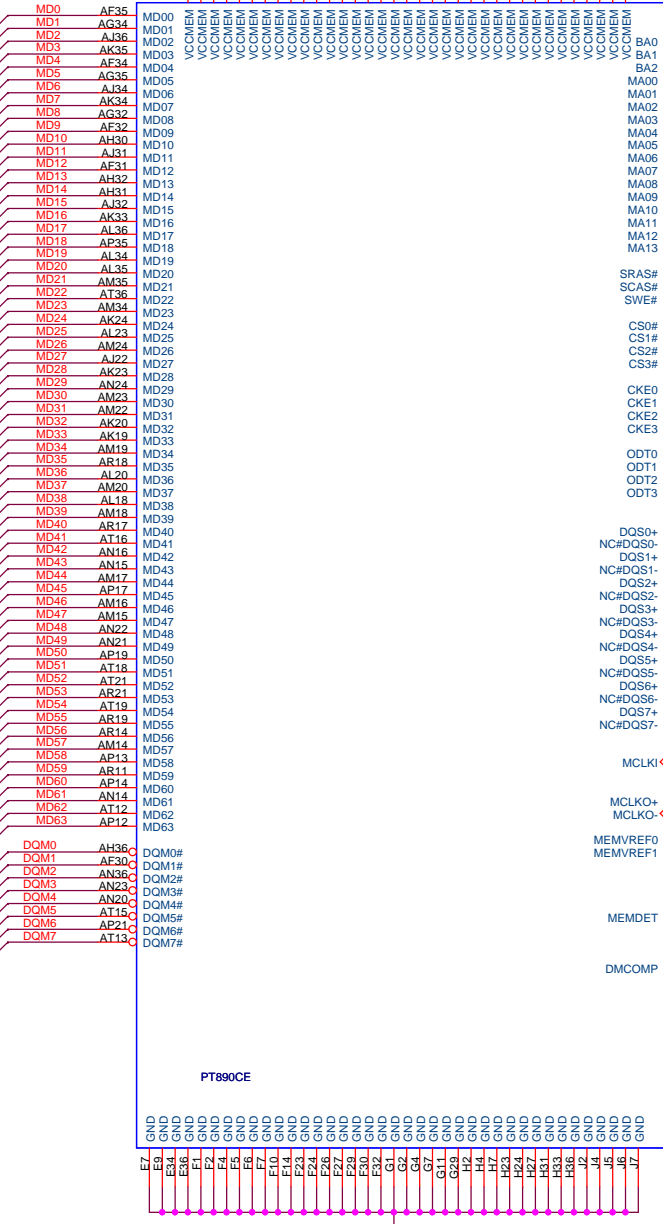






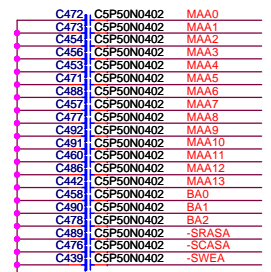
[13] MD[0:63]

[13] DQM[0:7]



Close to ball

Test Point
(Place near their respective balls of NB)

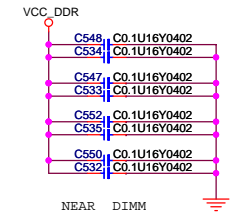


PULL DOWN GND OR PULL UP +1.8VDIMM

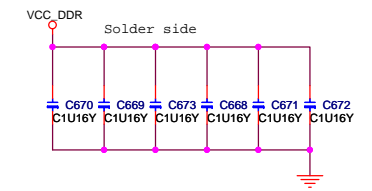
CLOSE TO DIMM

NOTE: DQS/DQS# => OTHER:W:S:W:OTHER=15:10:5:10:15

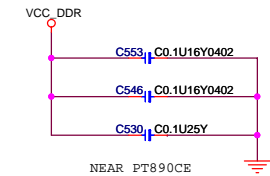
MCLKO+/- as short as passable
MCLKIT = DCLKx + 2 "



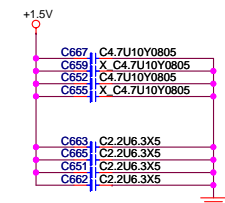
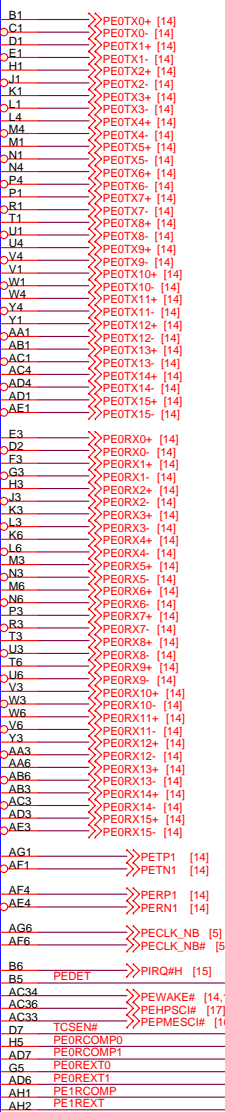
NEAR DIMM



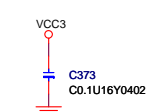
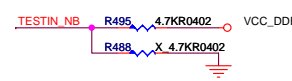
Solder side

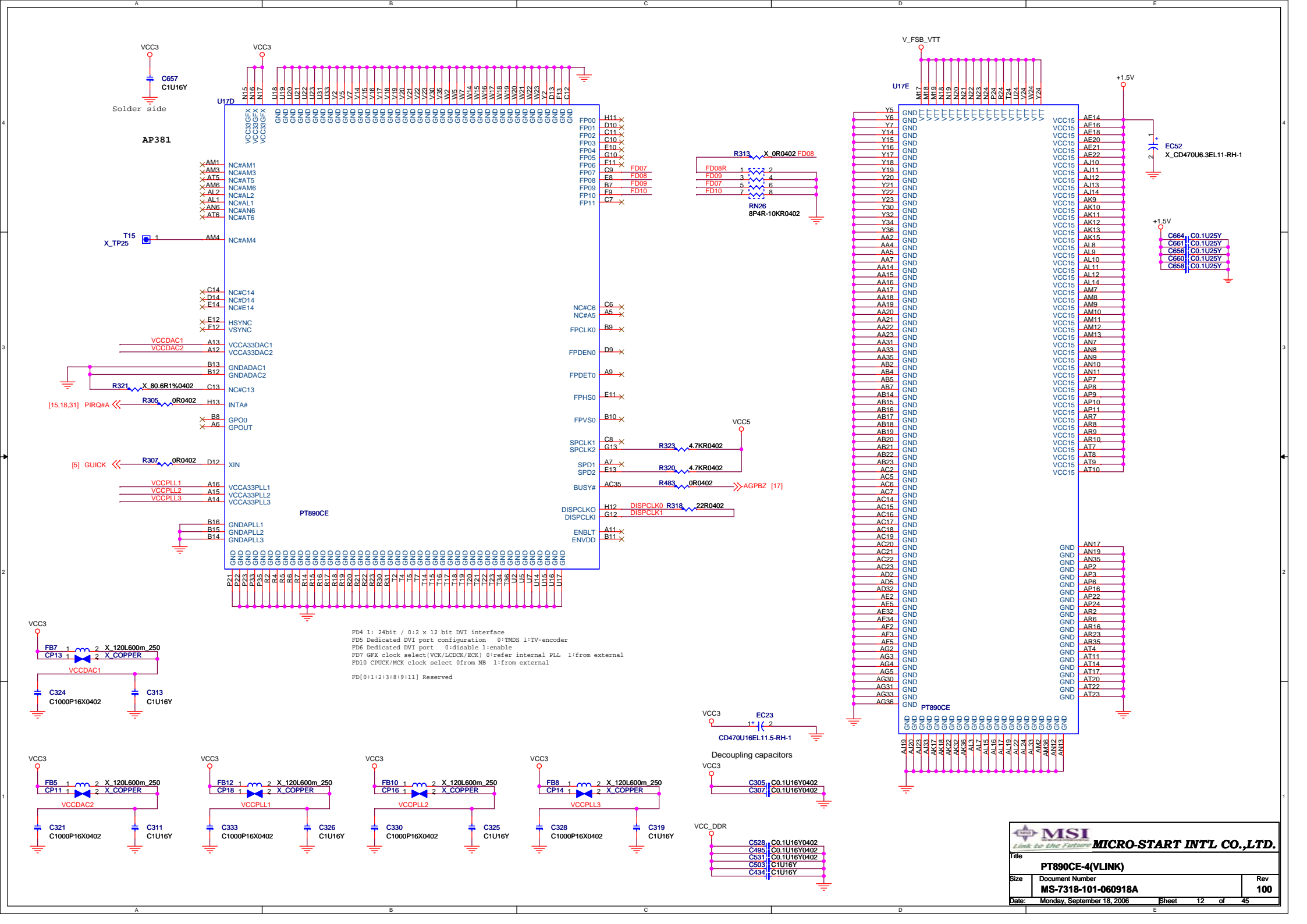


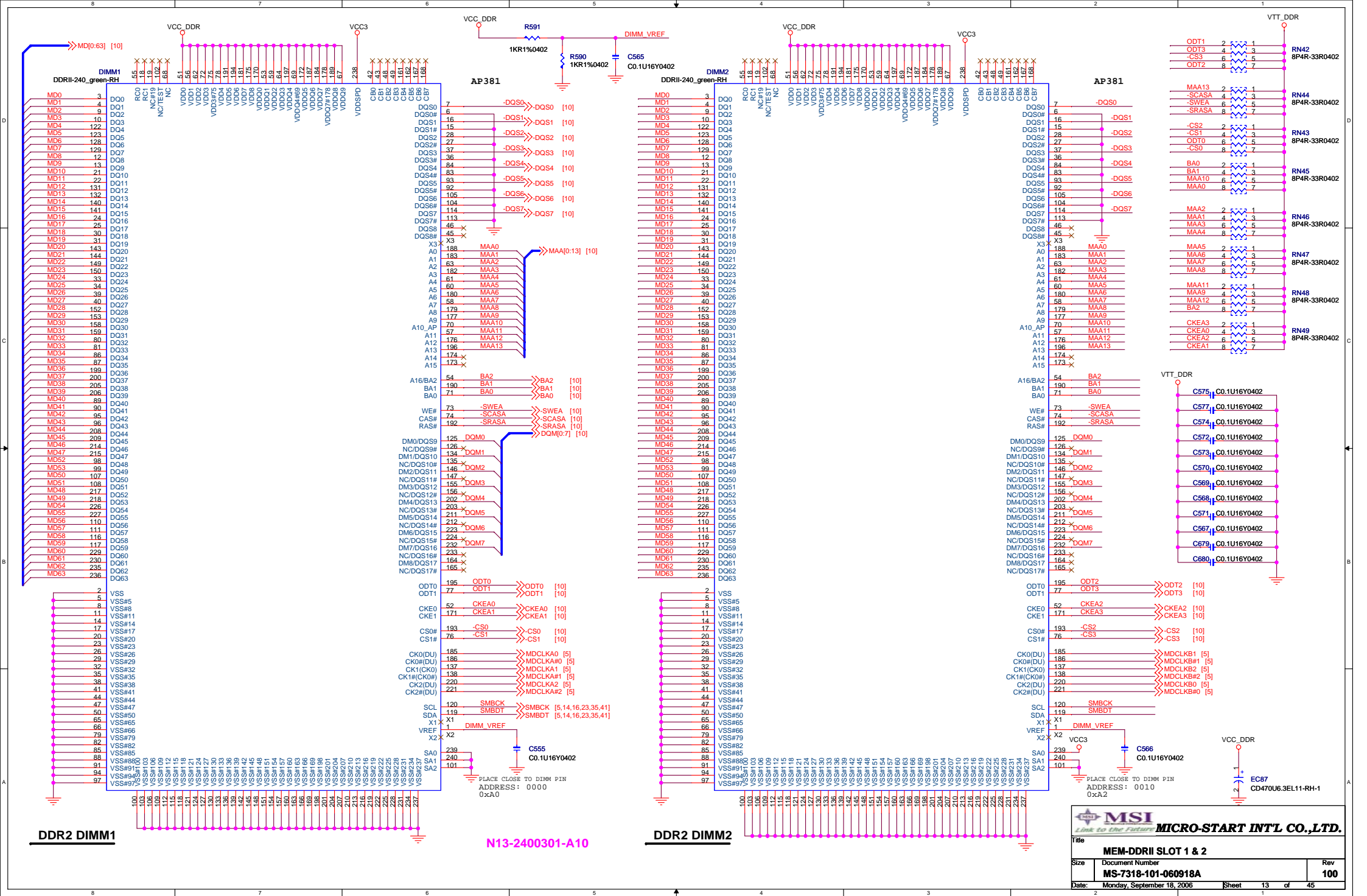
NEAR PT890CE

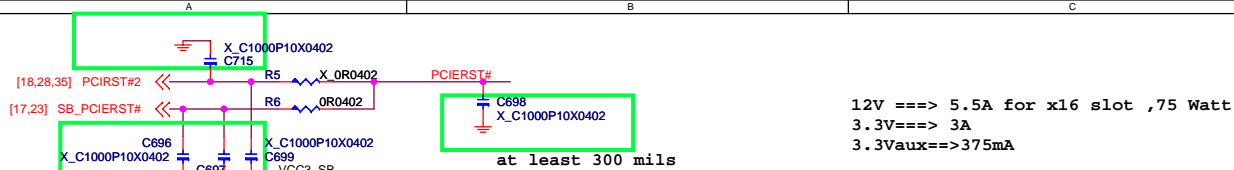


```
Strapping For NB_TEST Mode
TESTIN  BISTIN  RBF  WBF
1        1      x   x
Disable all TEST mode
```

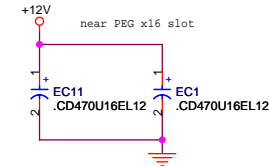
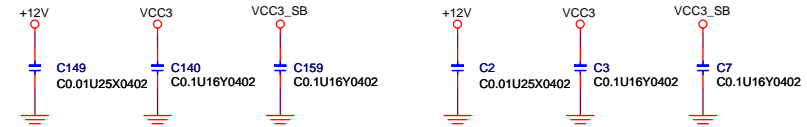
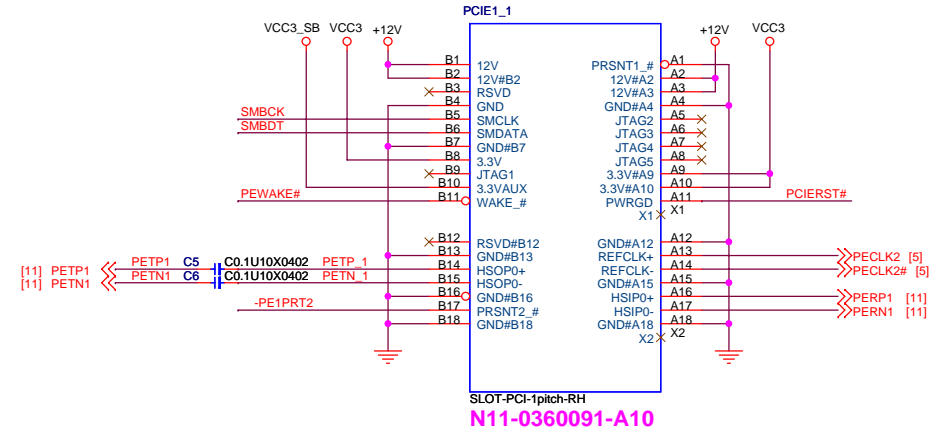






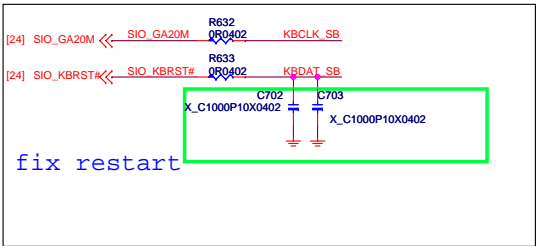


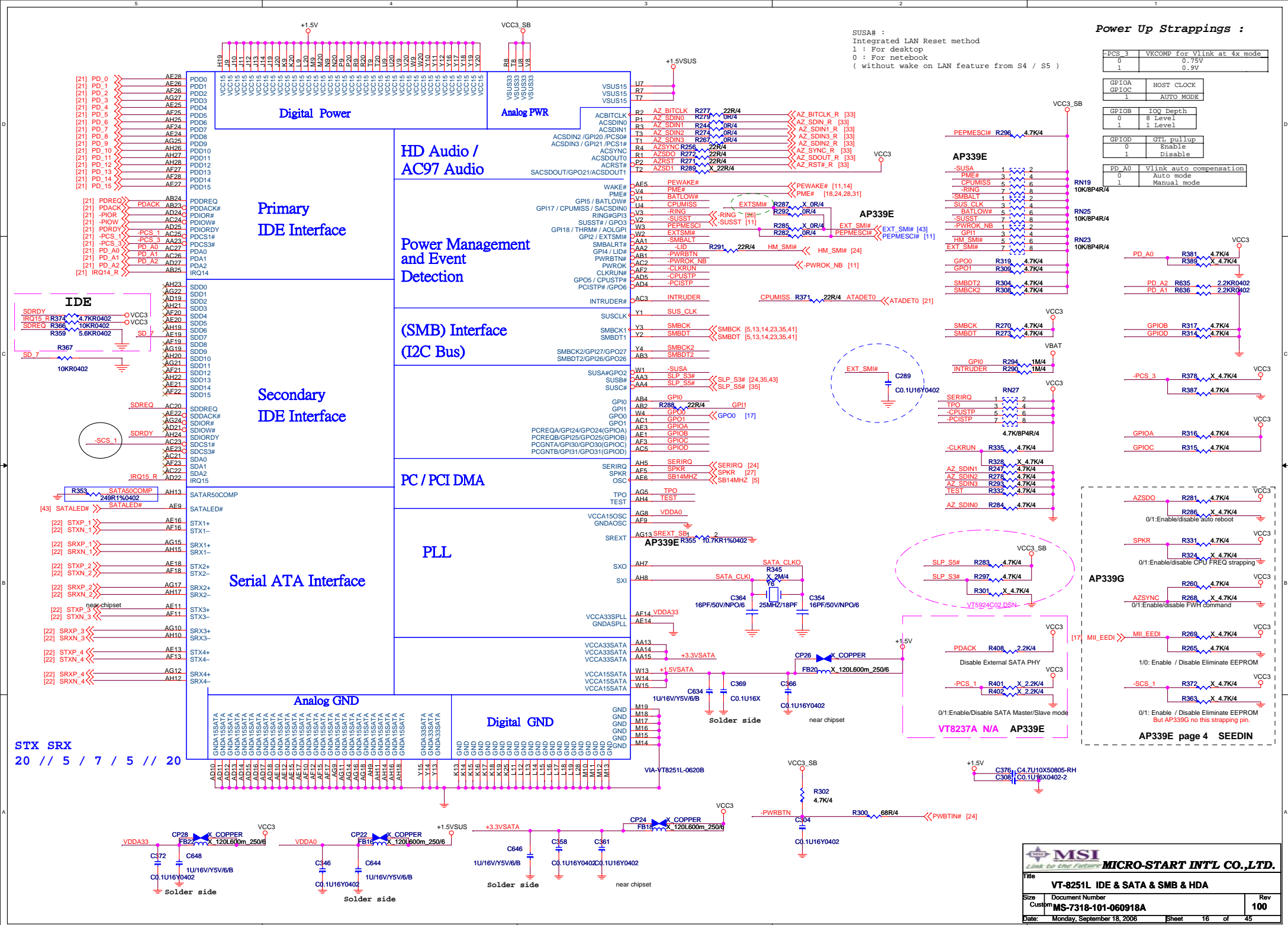
PCI EXPRESS 1-PORT 2

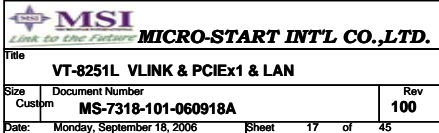


The system board designer determines the pull-up voltage

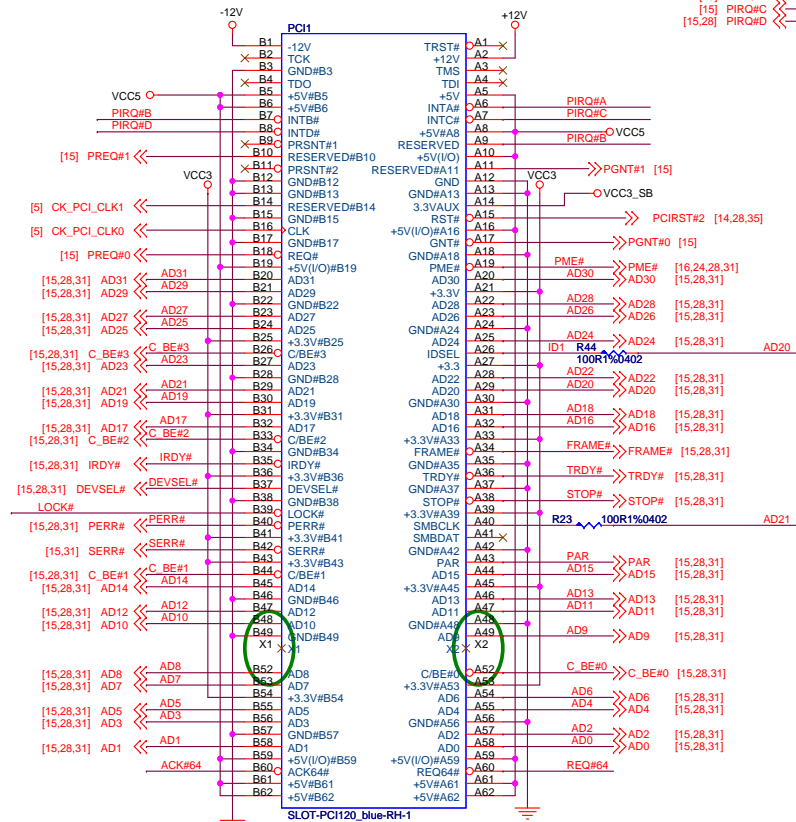
SLOT-PCI164-RH
N11-1640281-K06







PCI SLOT 1 (BLUE)

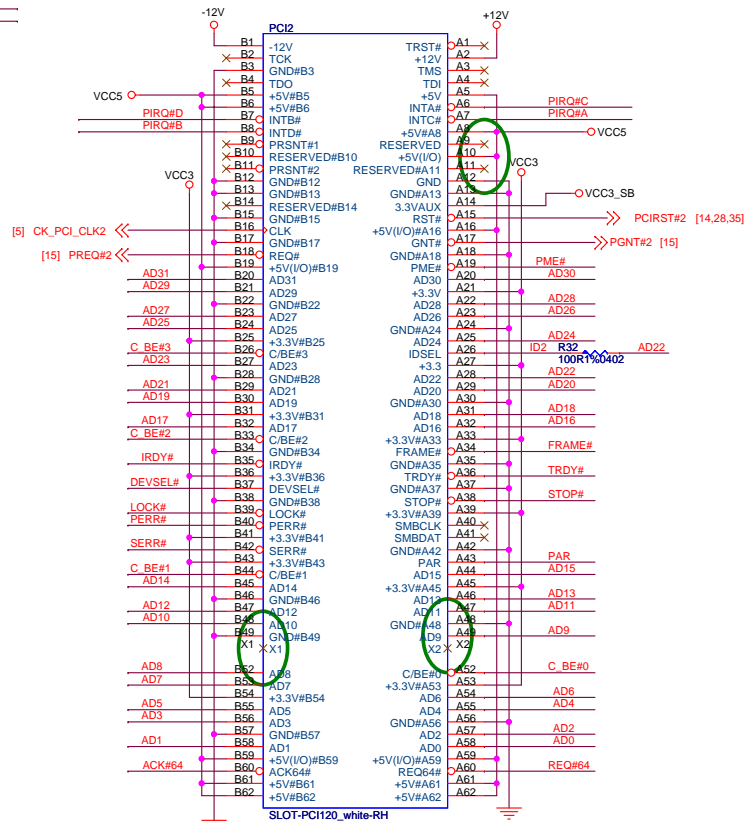


SLOT-PCI120_blue-RH-1

MEDION

IDSEL = AD20
MASTER = PREQ#0
PIRQ#A
CK_PCI_CLK0

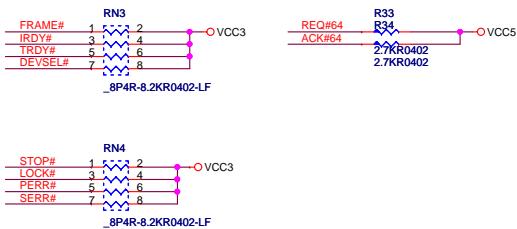
PCI SLOT 2



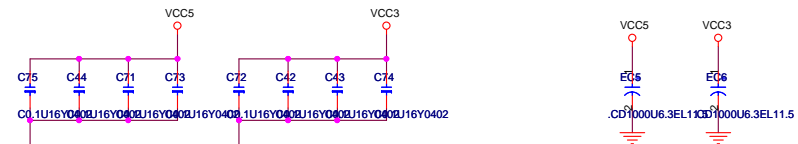
SLOT-PCI120_white-RH

IDSEL = AD22
MASTER = PREQ#2
PIRQ#C
CK_PCI_CLK2

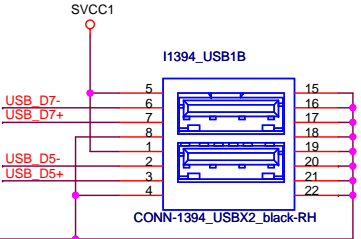
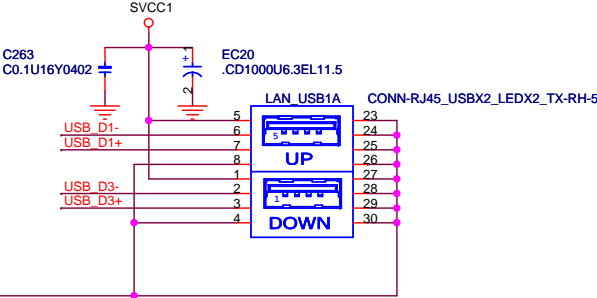
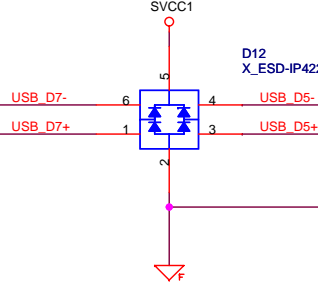
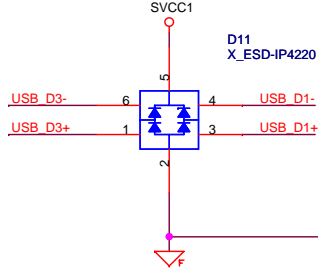
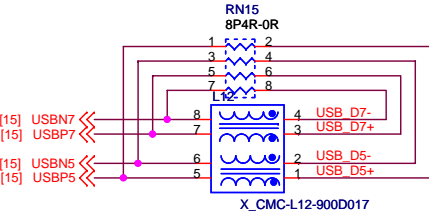
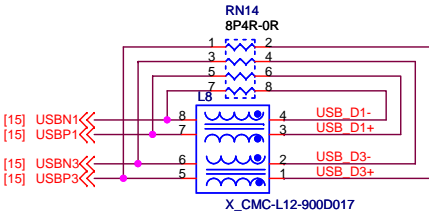
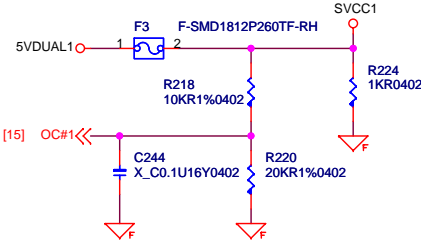
PCI PULL-UP / DOWN RESISTORS

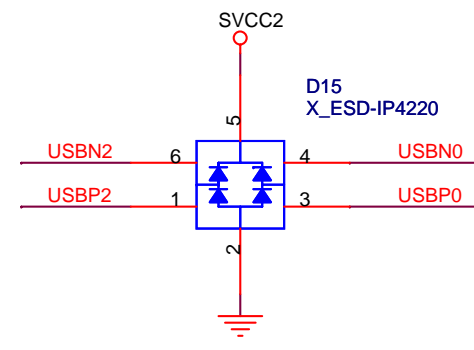
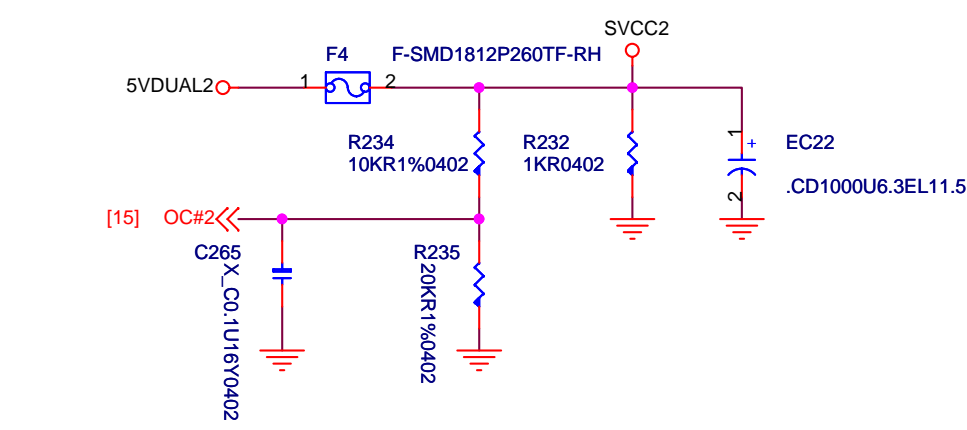


PCI SLOT DECOUPLING CAPACITORS

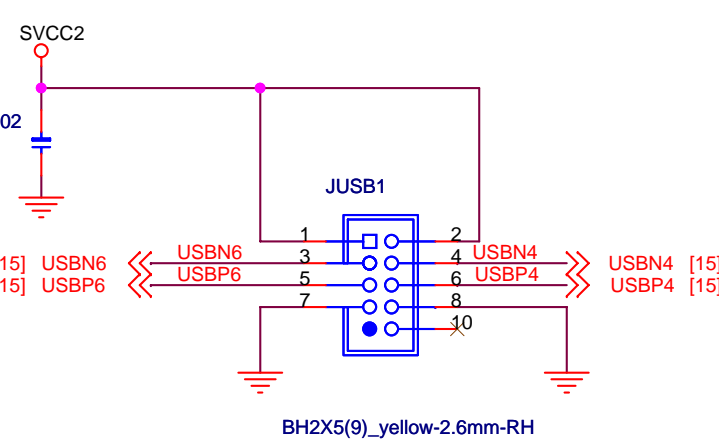
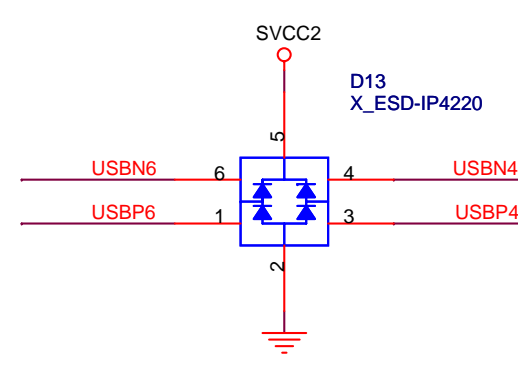
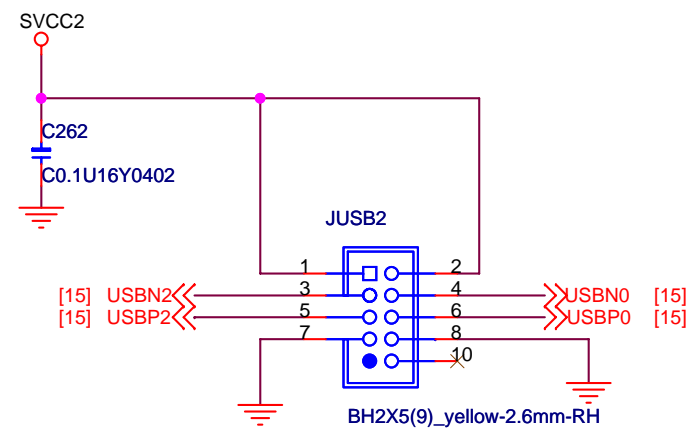



USB Rear Connector





JUSB1, JUSB2	
PIN1	VCC#1
PIN2	VCC#2
PIN3	USB0-
PIN4	USB1-
PIN5	USB0+
PIN6	USB1+
PIN7	GND7
PIN8	GND8
PIN9	KEY
PIN10	USBOC



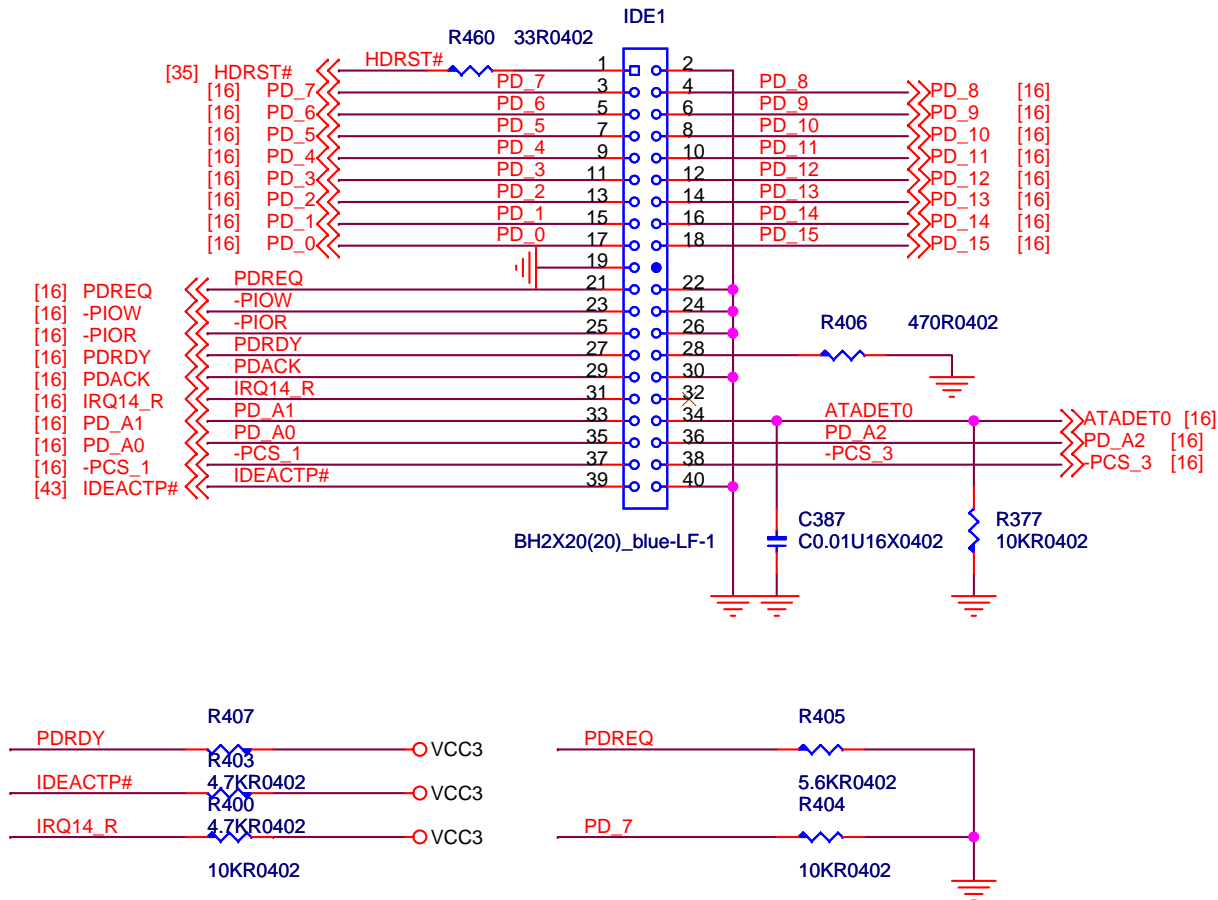


MSI
MICRO-STAR INTERNATIONAL
Link to the Future

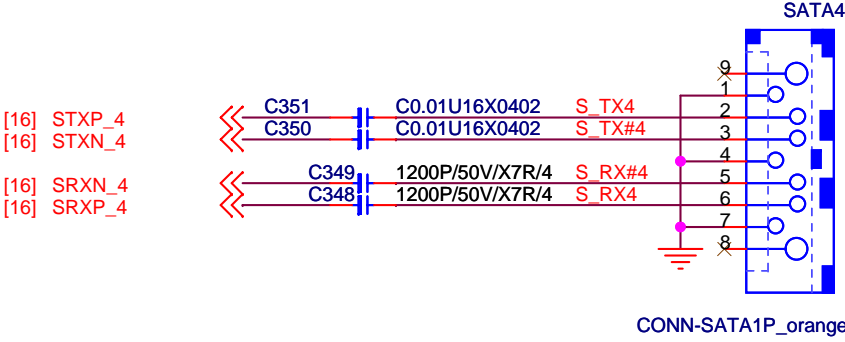
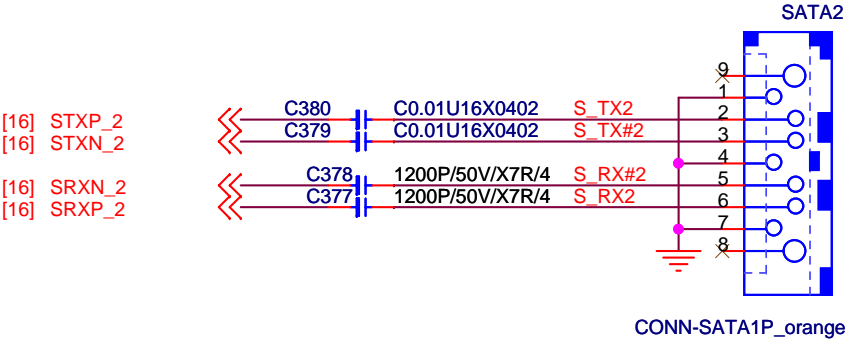
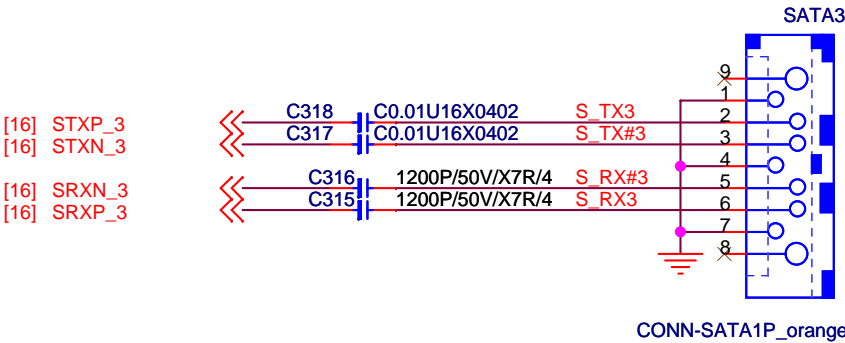
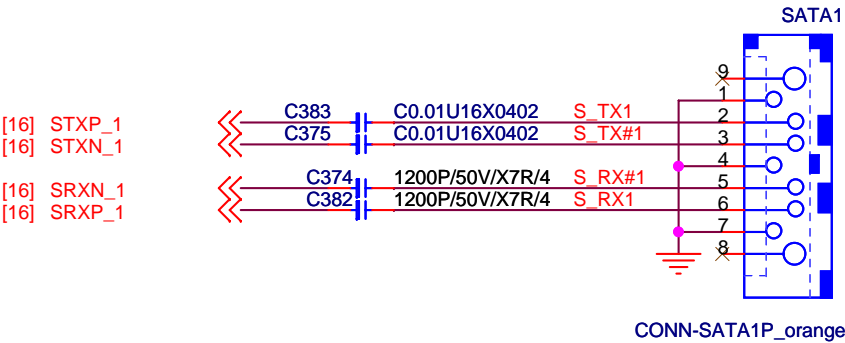
MICRO-STAR INT'L CO.,LTD.


Title		
USB Connectors -- Front		
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IDE Connector



SATA Connector





MSI

MICRO-STAR INTERNATIONAL

Link to the Future

MICRO-STAR INT'L CO.,LTD.

Title

SATA & IDE CONNECTOR

Size

Document Number

MS-7318-101-060918A

Rev

100

Date:

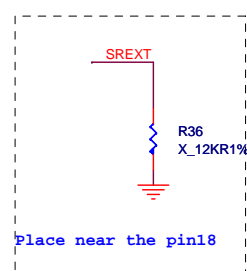
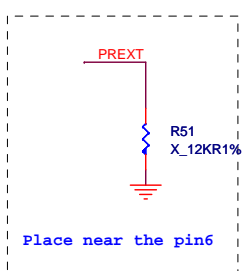
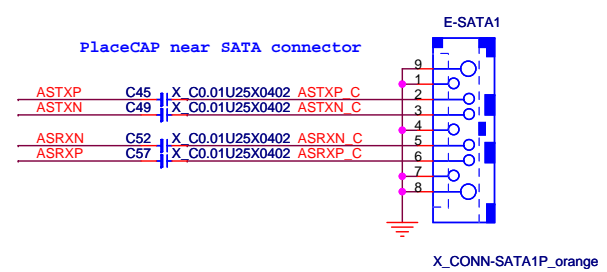
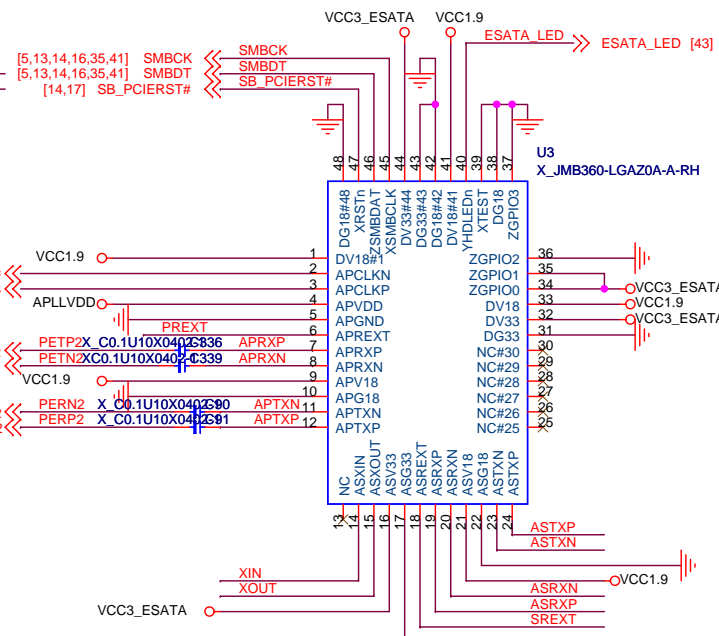
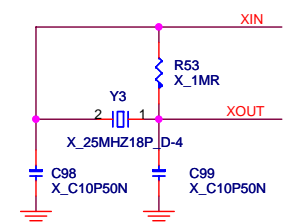
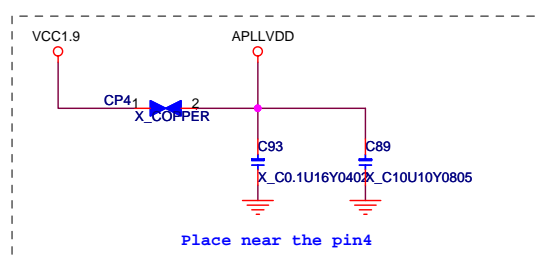
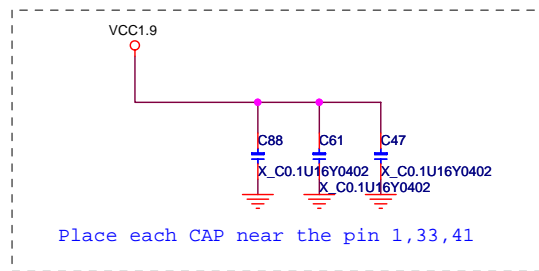
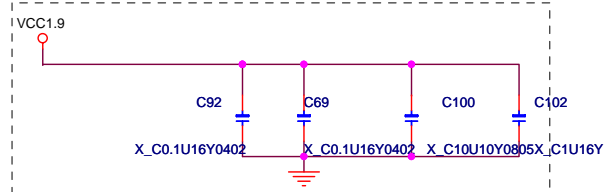
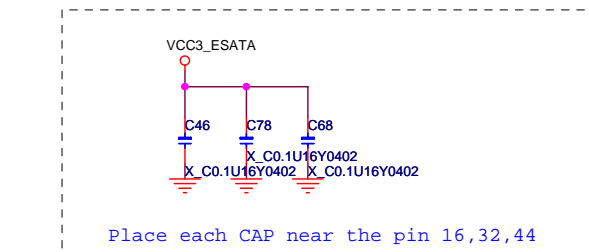
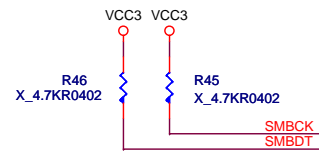
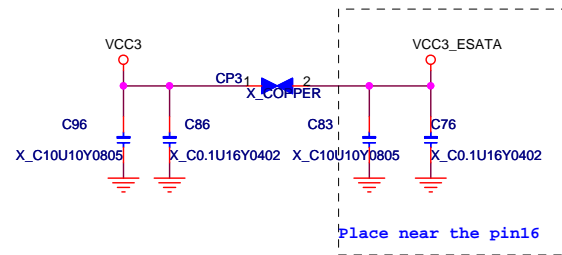
Monday, September 18, 2006

Sheet

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of

45



Micro Star Restricted Secret		
Title	e-SATA	Rev 100
Document Number	MS-7318-101-060918A	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, September 18, 2006 Sheet 23 of 45

[illegible]

[24] SIO_VIN0 <<< SIO_VIN0

R166 56KR1%0402

+12V

R161 10KR1%0402

[24] SIO_VIN2 <<< SIO_VIN2

R172 22.1KR1%0402

VCC5

R167 10KR1%0402

[24] SIO_VCORE <<<

R147 10KR0402

VCCP

The schematic diagram illustrates the electrical connections for the THERMIDA and THERMDC components. The THERMIDA component is connected to the SIO_TMP_VREF signal via a resistor R124 (X_15KR1%0402). The THERMDC component is connected to the SIO_AGND signal via a capacitor CP6 (C2200P16X0402). The SIO_TMP_VREF and SIO_AGND signals are connected to the SIO_TMP input of the THERMIDA component. The SIO_TMP_VREF signal is also connected to the SIO_TMP_VREF input of the THERMIDA component. The SIO_AGND signal is also connected to the SIO_AGND input of the THERMIDA component. The SIO_TMP_VREF and SIO_AGND signals are connected to the SIO_TMP input of the THERMIDA component.

The schematic diagram illustrates the CPU fan control circuit. It features two fans: CPUFAN1 (X_BH1X3BP_white-RH) and CPU_FAN1 (BH1X4B_white-3.3mm-RH). The circuit includes several resistors (R102, R117, R125, R138, R150, R175), capacitors (EC13, C196), and diodes (D7, D6). Key components include the +12V power source, the BAS32L_LL34 diode, and the CD470U16EL11.5 capacitor. The output signals are labeled CPU_FANIN0 [24] and CPU_FANOUT0.

System FAN

The schematic diagram shows the electrical connections for the System FAN. A +12V supply is connected to a diode D6 (BAS32L_LL34) in series with a resistor R168 (4.7KR0402). The output of the diode is connected to the SYS_FAN1 pin of the BH1X3BP_white-RH fan. The fan's other pins are connected to ground. The fan's ground is also connected to the SYS_FANIN pin of the 27KR0402 resistor, which is connected to the SYS_FANIN pin of the 27KR0402 resistor. The SYS_FANIN pin is also connected to the SYS_FAN_PWR pin of the EC15 CD470U16EL11.5 fan. The SYS_FAN_PWR pin is connected to the SYS_FAN_SEN pin of the 10KR0402 resistor, which is connected to the SYS_FAN_SEN pin of the 10KR0402 resistor. The SYS_FAN_SEN pin is connected to the SYS_FAN_SEN pin of the 10KR0402 resistor, which is connected to the SYS_FAN_SEN pin of the 10KR0402 resistor.

VBAT_SIO

R42 2MR0402

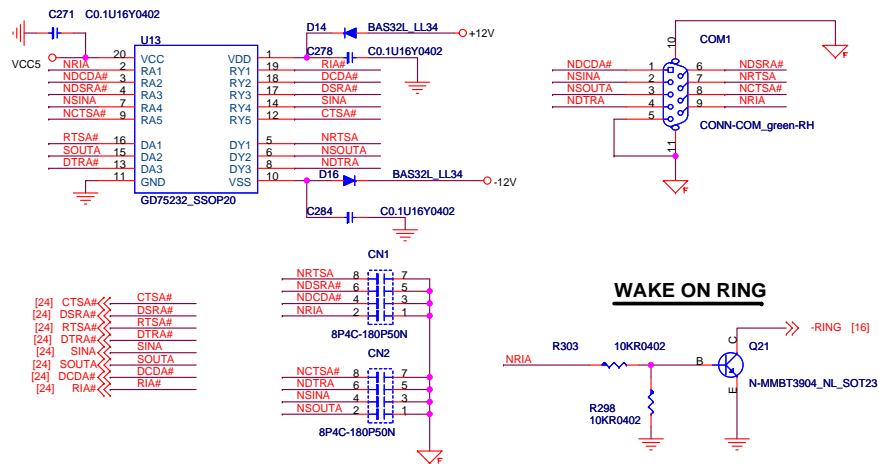
J3

1 2

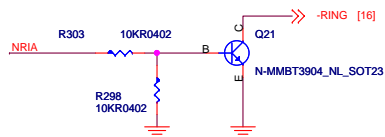
SIO_CASEOPEN# [24]

X_H1X2_black-15u-in-RH

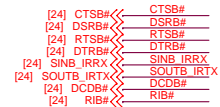
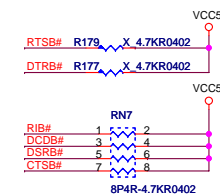
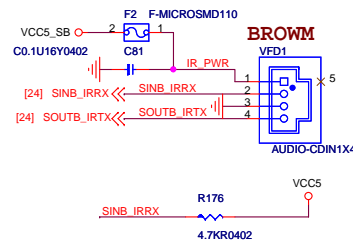
SERIAL PORT 1



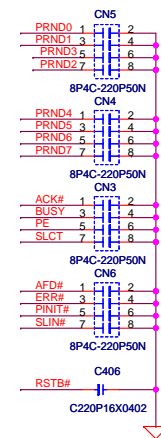
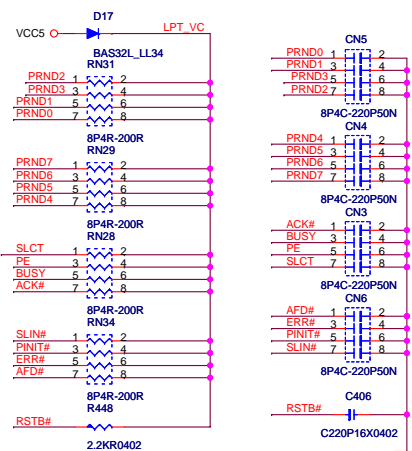
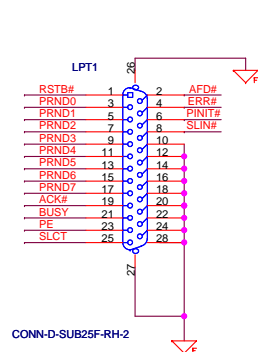
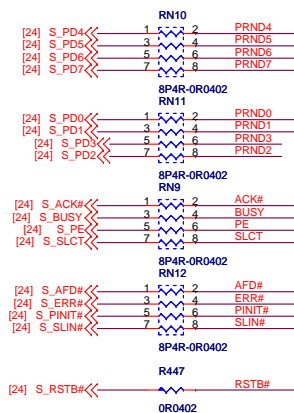
WAKE ON RING



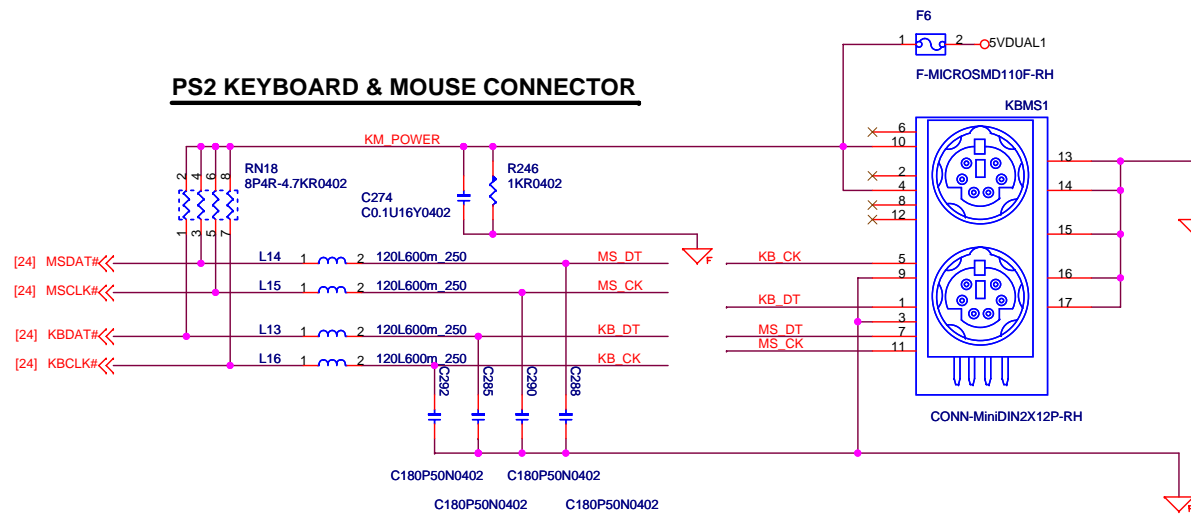
Front LCD (SERIAL PORT 2)



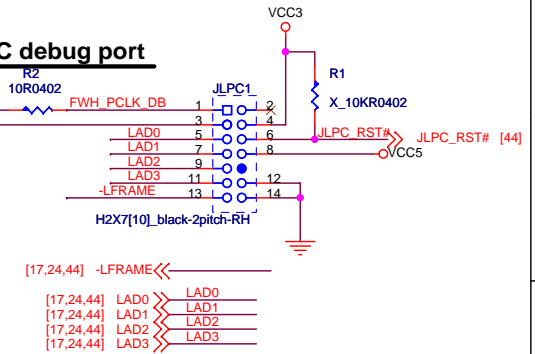
PARALLAL PORT



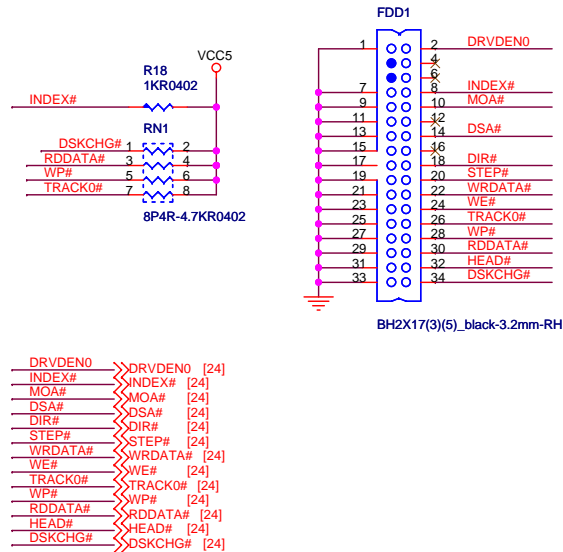
PS2 KEYBOARD & MOUSE CONNECTOR



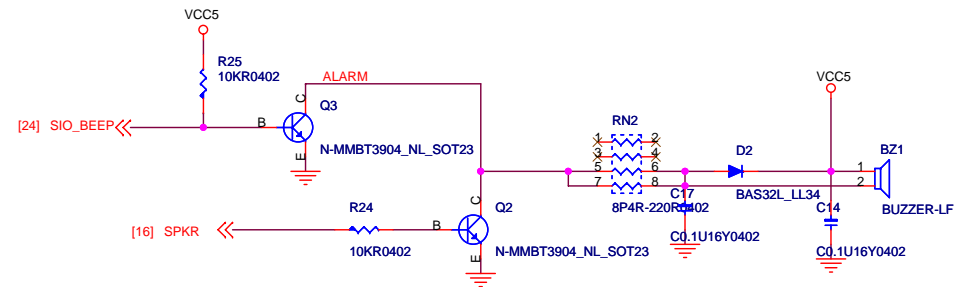
LPC debug port



FLOPPY CONNECTOR

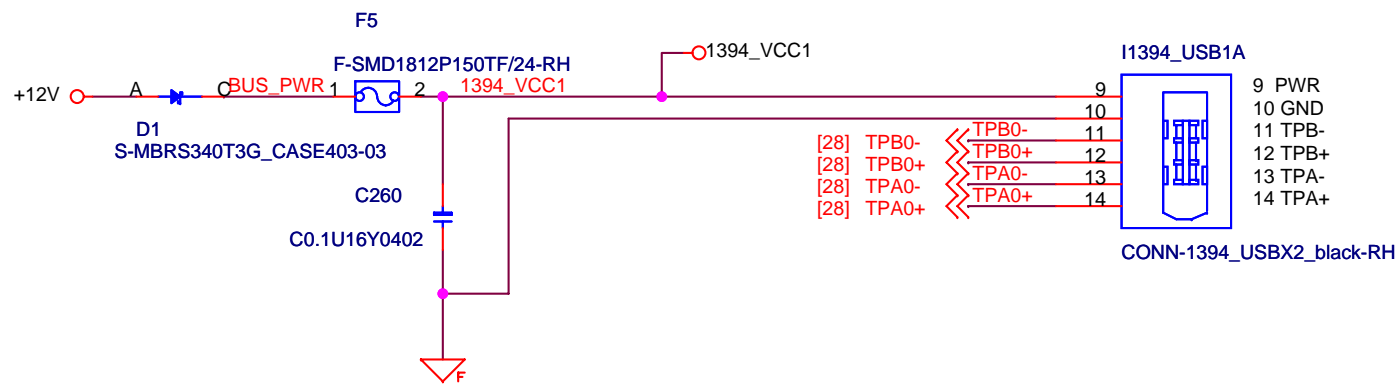


BUZZER

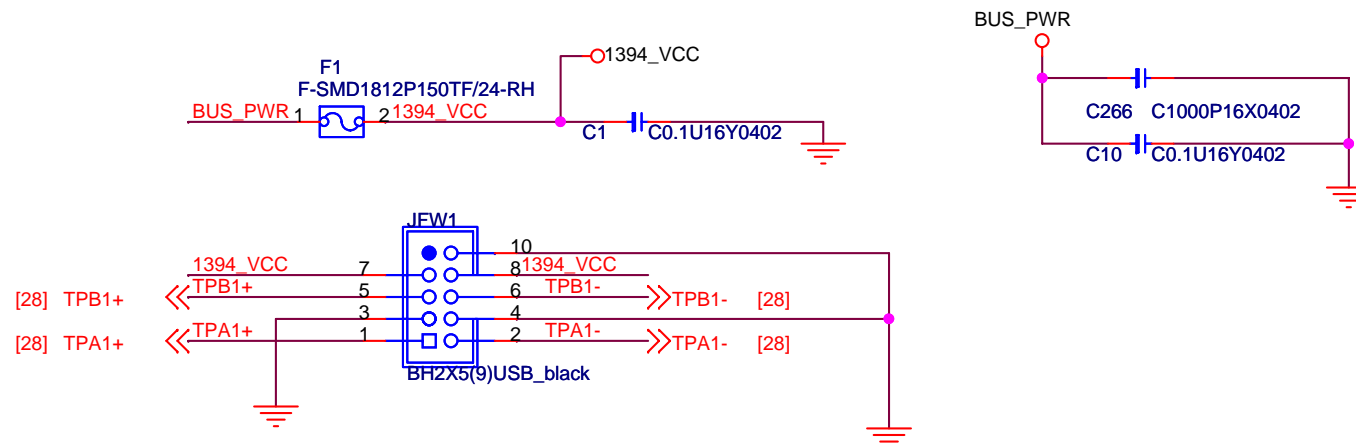


MICRO-START INT'L CO.,LTD. <i>Link to the Future</i>		
Title: SIO_KB, FDD, LPC Debug Port		
Size: B	Document Number: MS-7318-101-060918A	Rev: 100
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REAR 1394 PORT



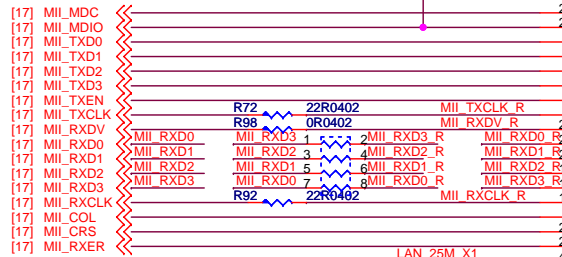
FRONT 1394 PORT



Title		
1394 PORT		
Size	Document Number	Rev
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PHY HW CONFIG

PHY ADDRESS = 00001
ASYMMETRIC PAUSE ENABLED
AUTO-NEG, ADVERTISE ALL MODES, PREFER MASTER
RGMII ON COPPER
ENERGY DETECT & COPPER/FIBER SELECT DISABLED
MDC/MIDIO MANAGEMENT SELECTED



U7

RTL8201BL /
RTL8201CL /
RTL8201CL+

LED0/PHYAD0
LED1/PHYAD1
LED2/PHYAD2
LED3/PHYAD3
LED4/PHYAD4

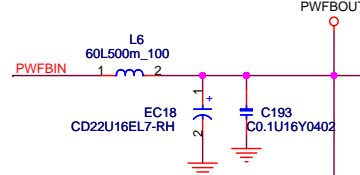
PWFBIN
DVDD33
DVDD33

RTL8201CL

[17] MII_RST#

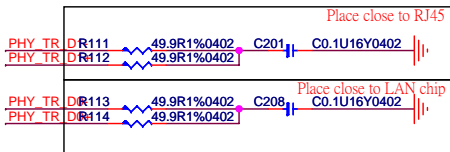
If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CL+ and MAC. In this kind of application, discard R532 and retain other components for one resetting upon power up.

PWFBOUT is 1.8V voltage outpt.
EC6 TCAP 22uF change ECAP 100uF
Place L11 close to PWFBOUT



RTL8201BL : R74(NC)
RTL8201CL : R47(0 ohm)
RTL8201CL+ : R47(0 ohm)

MII_PD# [17]



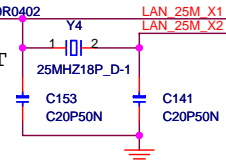
Place close to RJ45
Place close to LAN chip

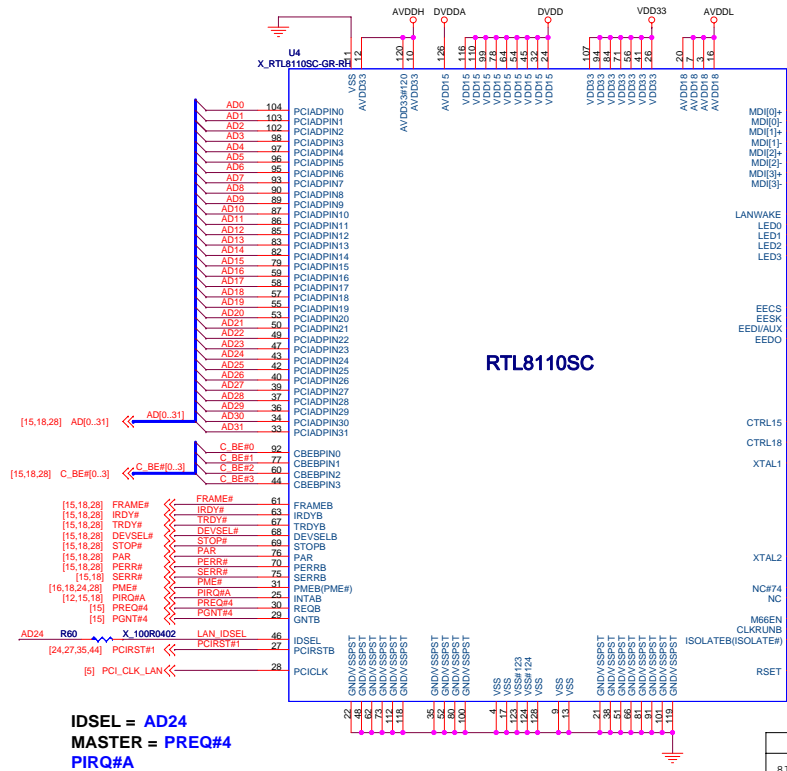


Hardwire Configuration network:

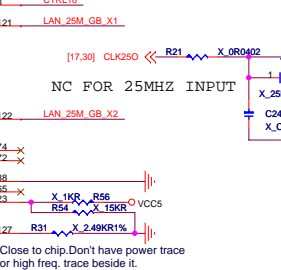
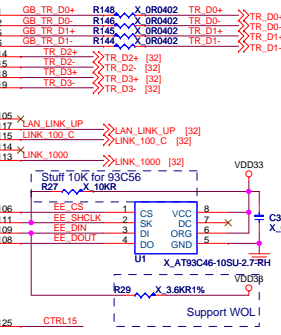
1. This configuration shows
Enable: Auto negotiation, Full duplex, 100Mbps,
Link Down Power Saving, MII interface
Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected to VDD or GND directly.

NC FOR 25MHZ INPUT

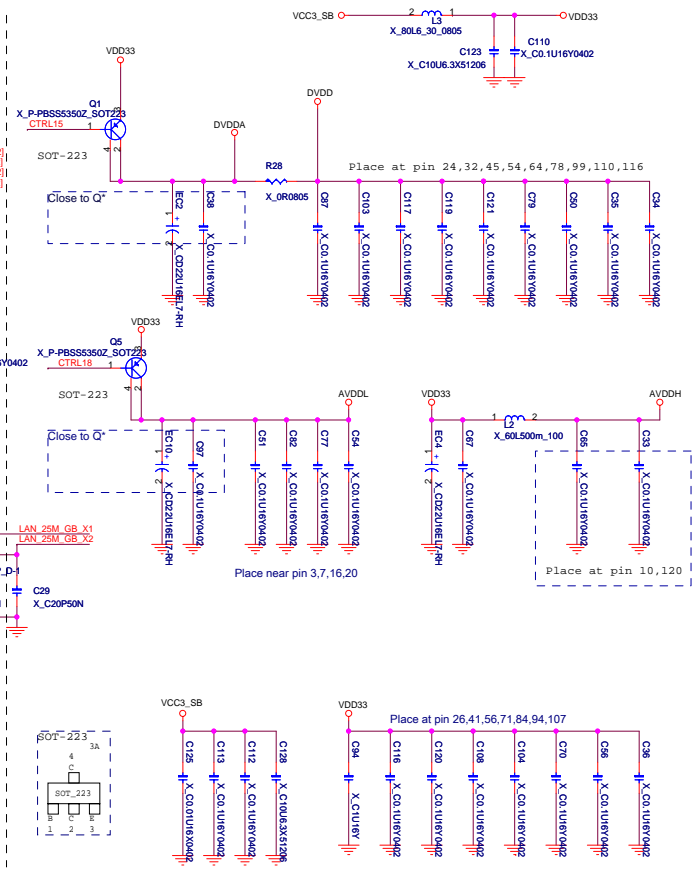




1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.



	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8110SC	1.5V	1.5V	1.8V	3.3V	3.3V



MICRO-START INT'L CO.,LTD.

RTL-8110SC

Size

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RJ45 Connector (with transformer)

LAN Interface

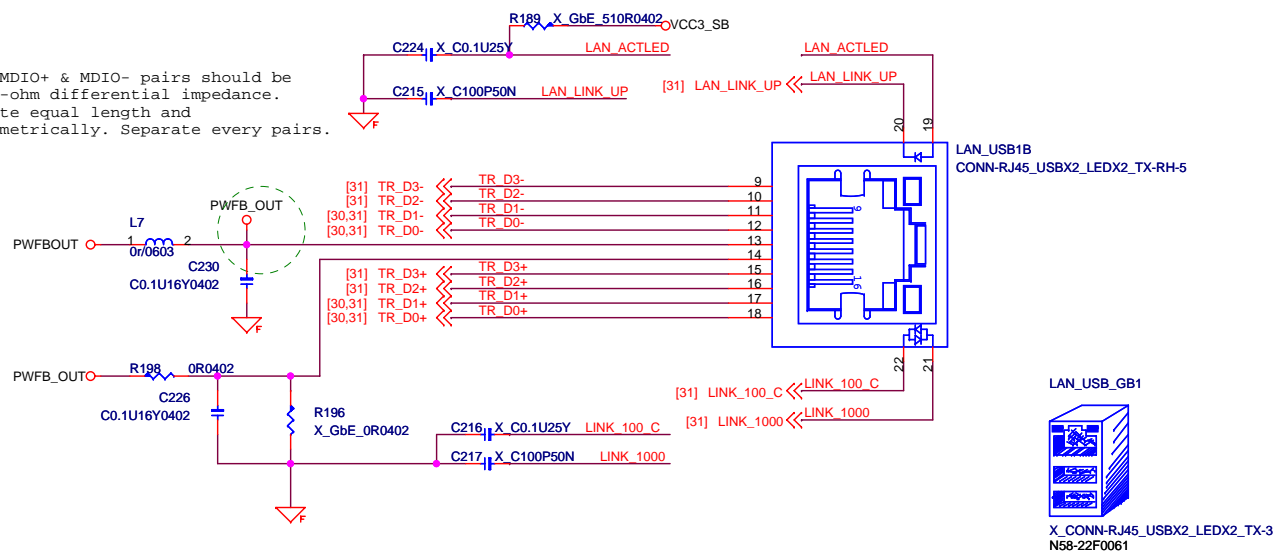
Diff. Trace width 8 mils & 8 mils space.

Diff. & other space 40 mils.

Length matching: < 10 mils

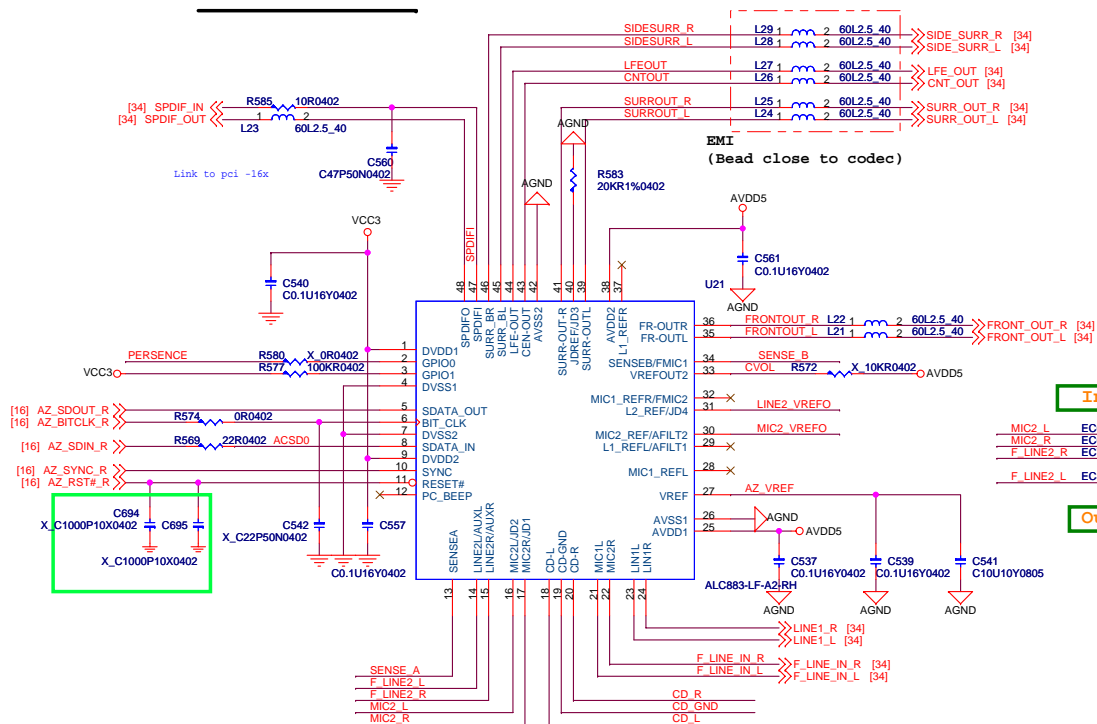
Ttrace length 0" to 2"

1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.

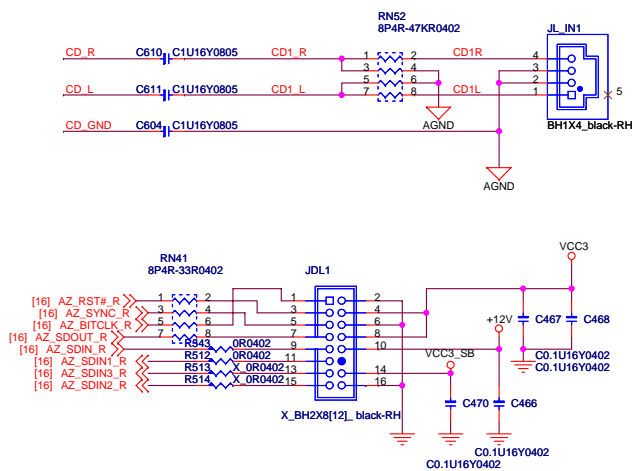


1G N58-22F0211-S42 : LED RoHS
10/100 N58-18F0081-S42 : Non LED and RoHS

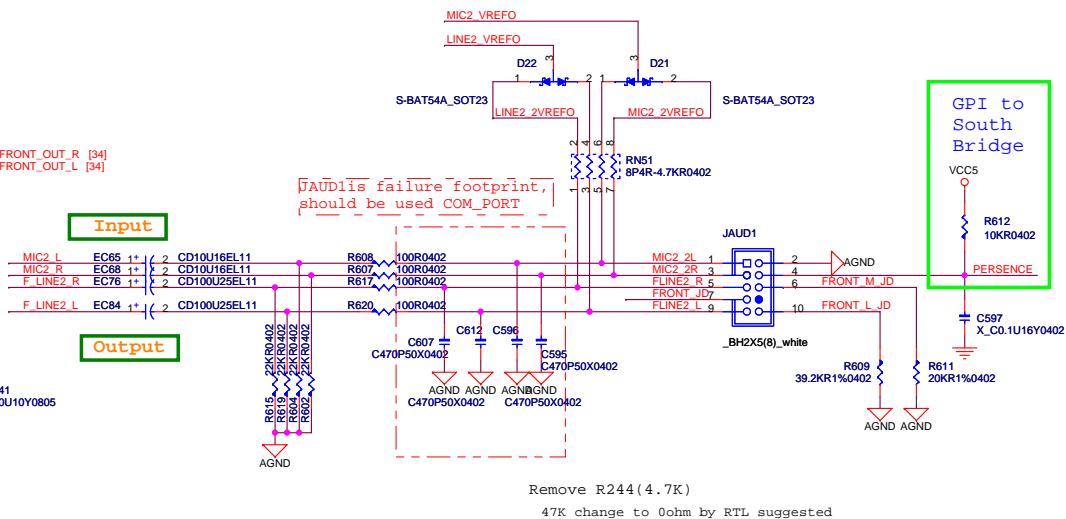
ALC888 CODEC



RCA Line-in (Input)

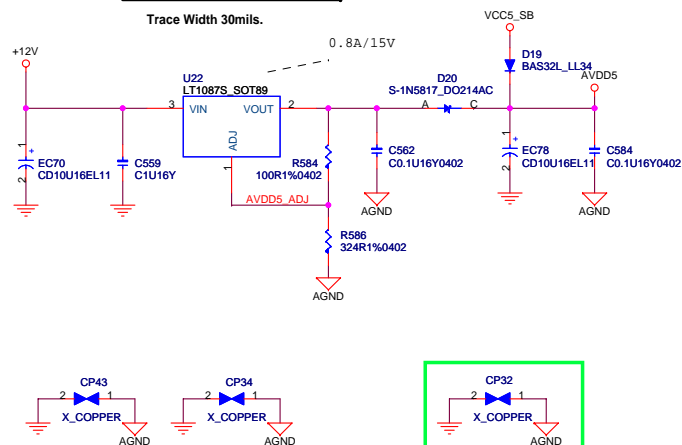


FRONT AUDIO

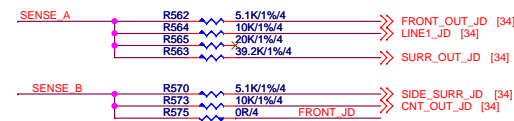


AUDIO CODE REGULATORS

Trace Width 30mils.

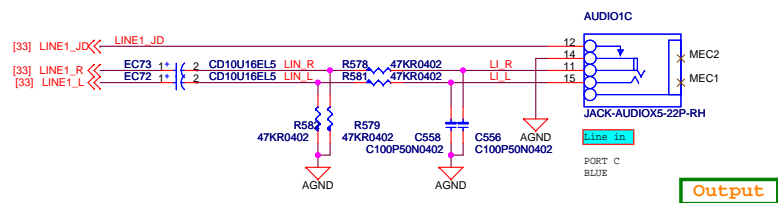
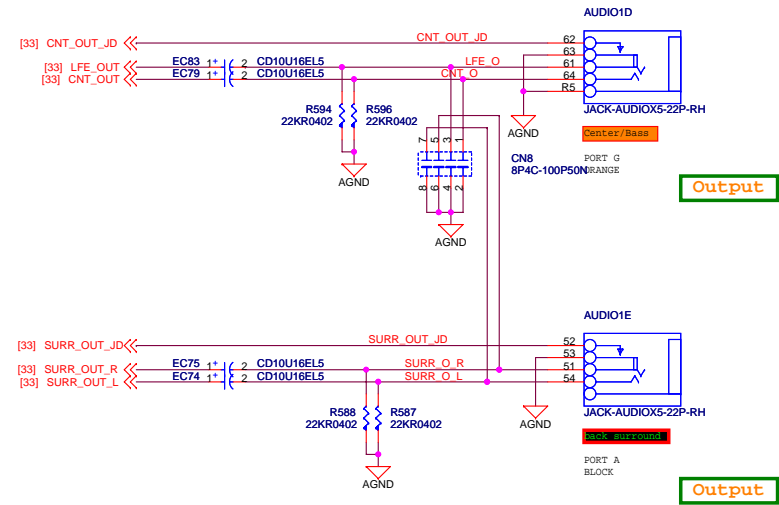
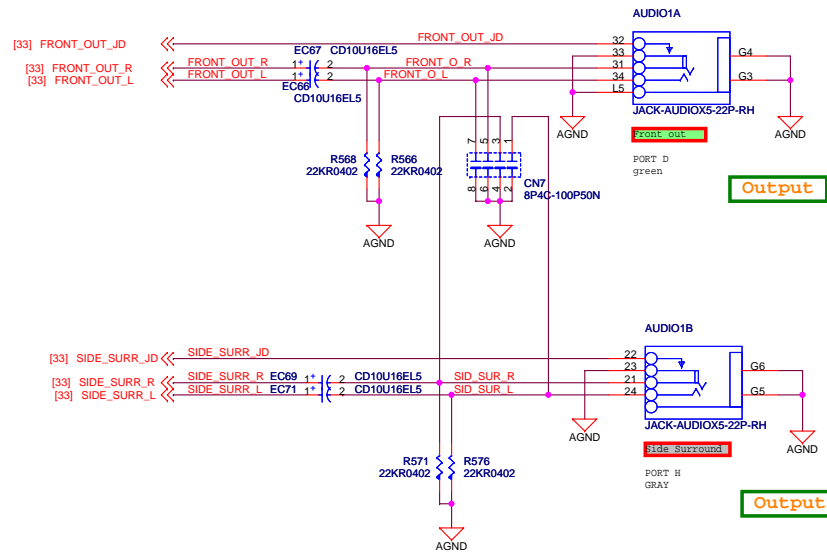


ALC883/888 JACK DETECT

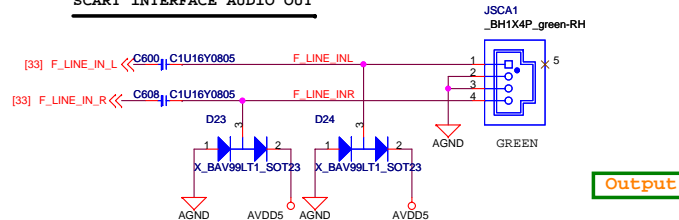


Closer to Codec.

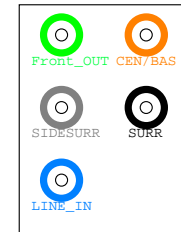
Audio Connector



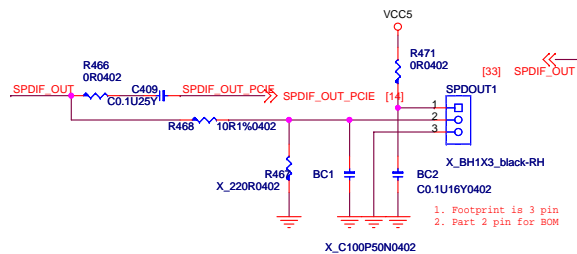
SCART INTERFACE AUDIO OUT



5-JACK

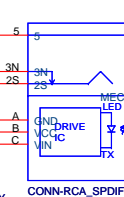


SPDIF OUT for HDMI of VGA

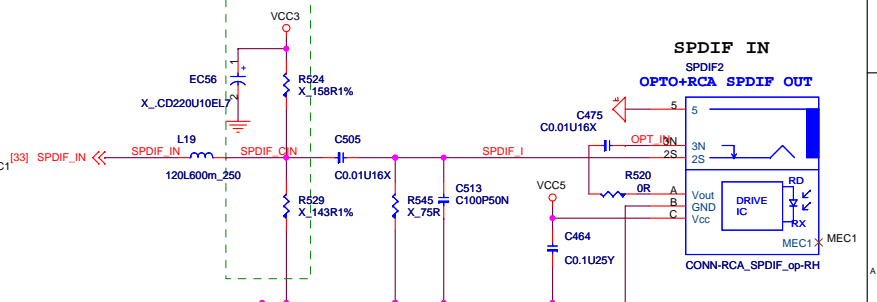


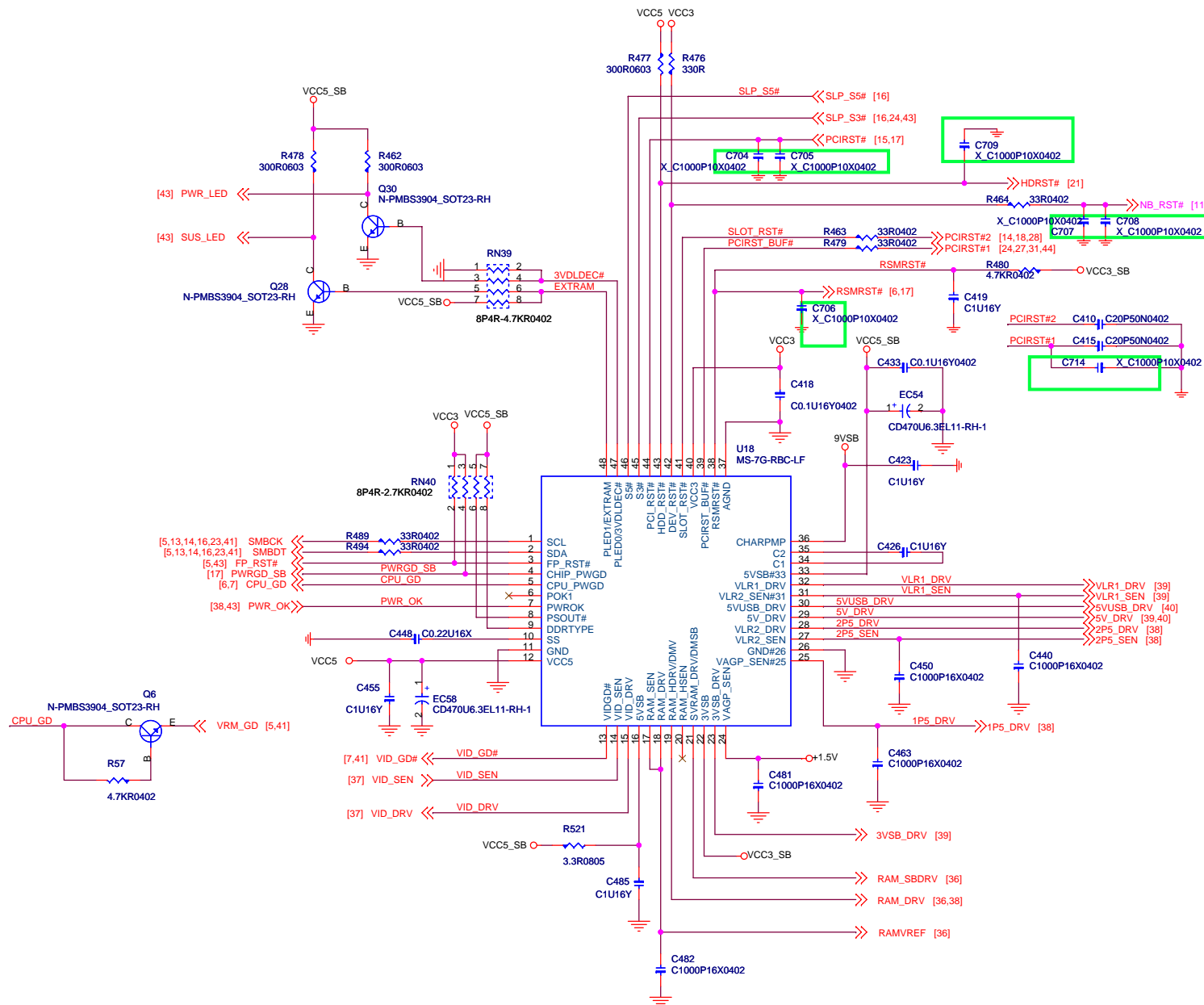
680pF change to 100pF by RTL suggested

SPDIF OUT

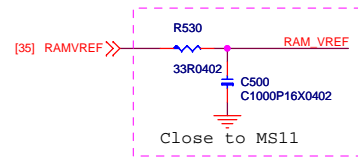
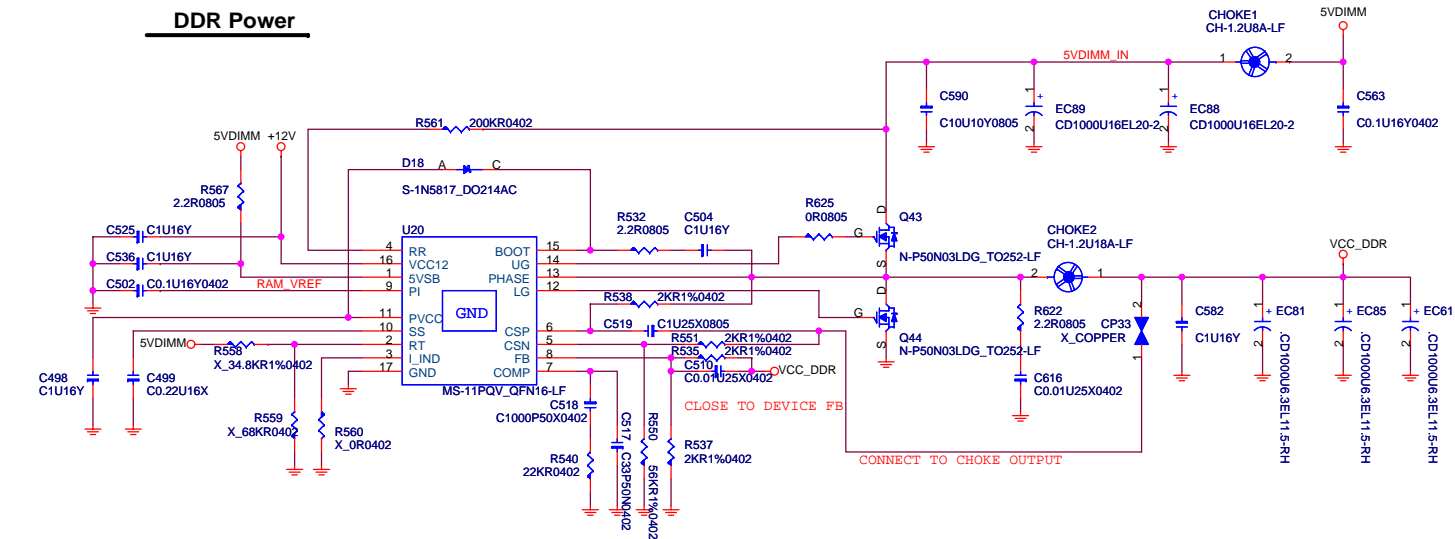


FOR alc880

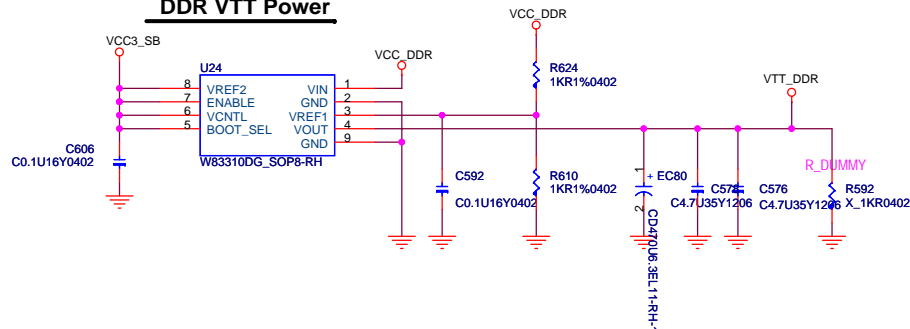




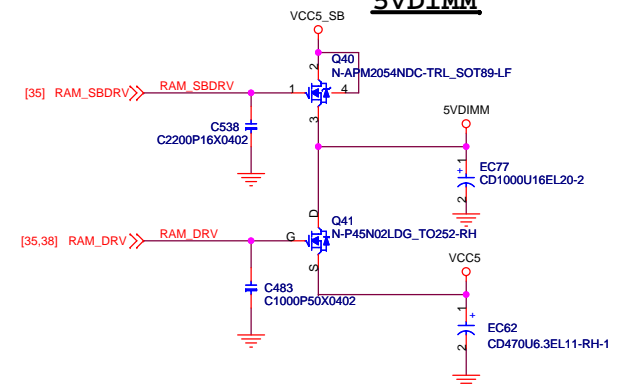
DDR Power



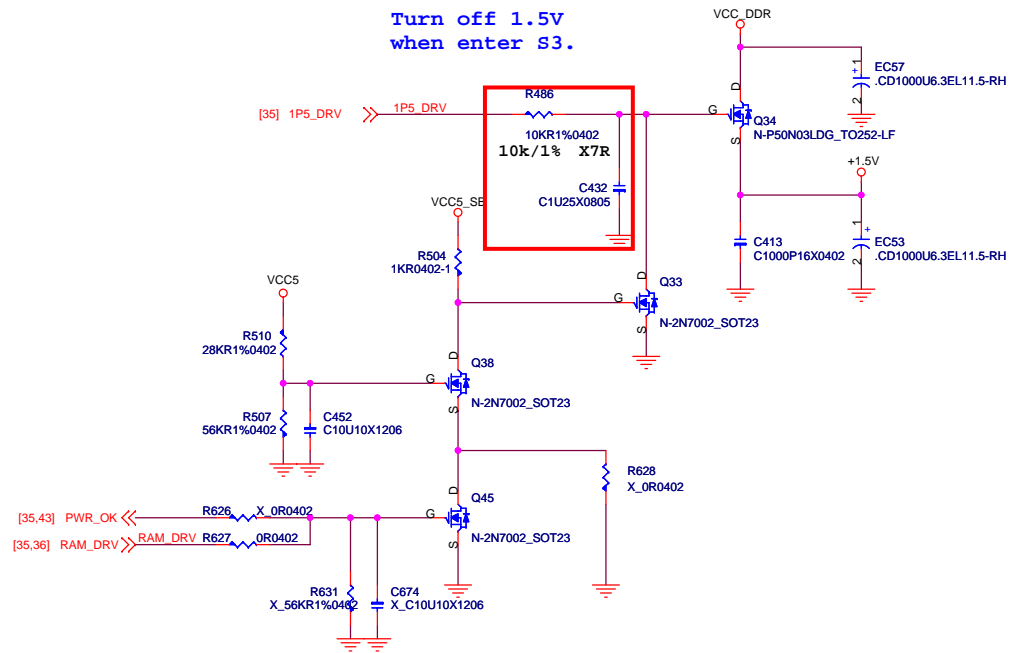
DDR VTT Power

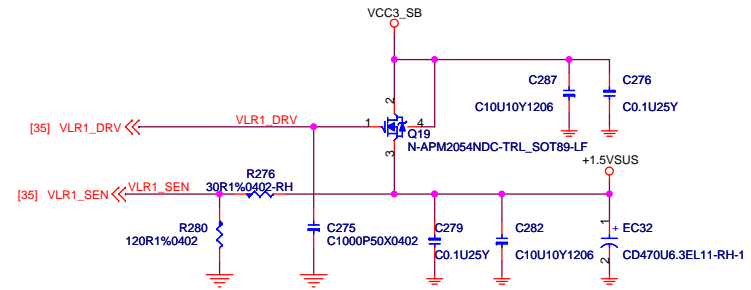
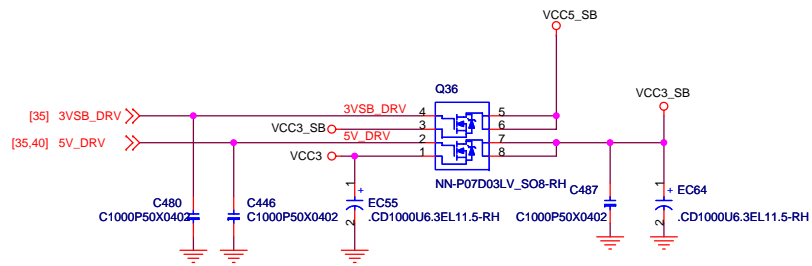


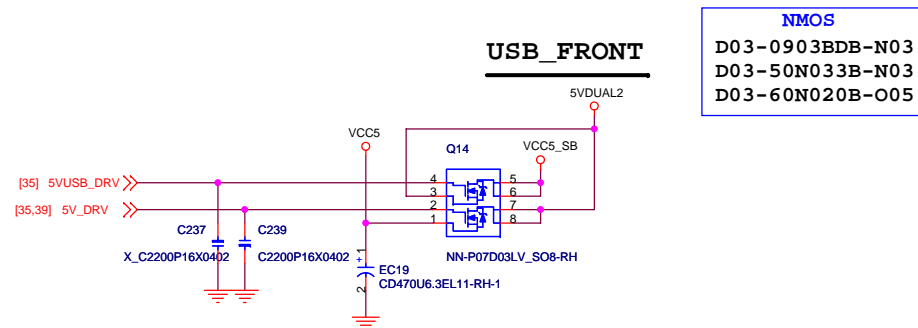
5VDIMM



Turn off 1.5V
when enter S3.

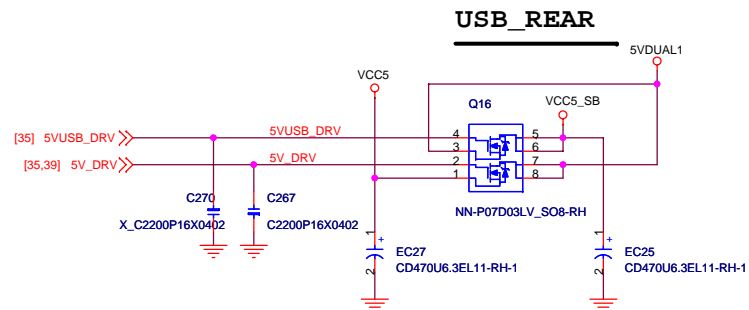
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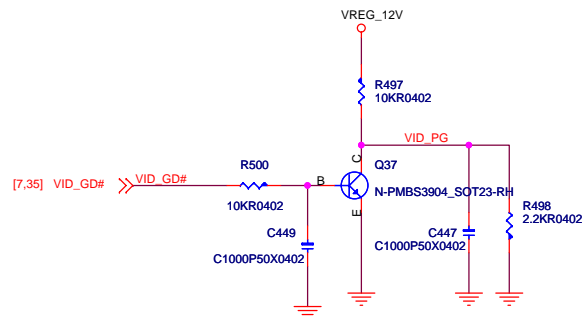
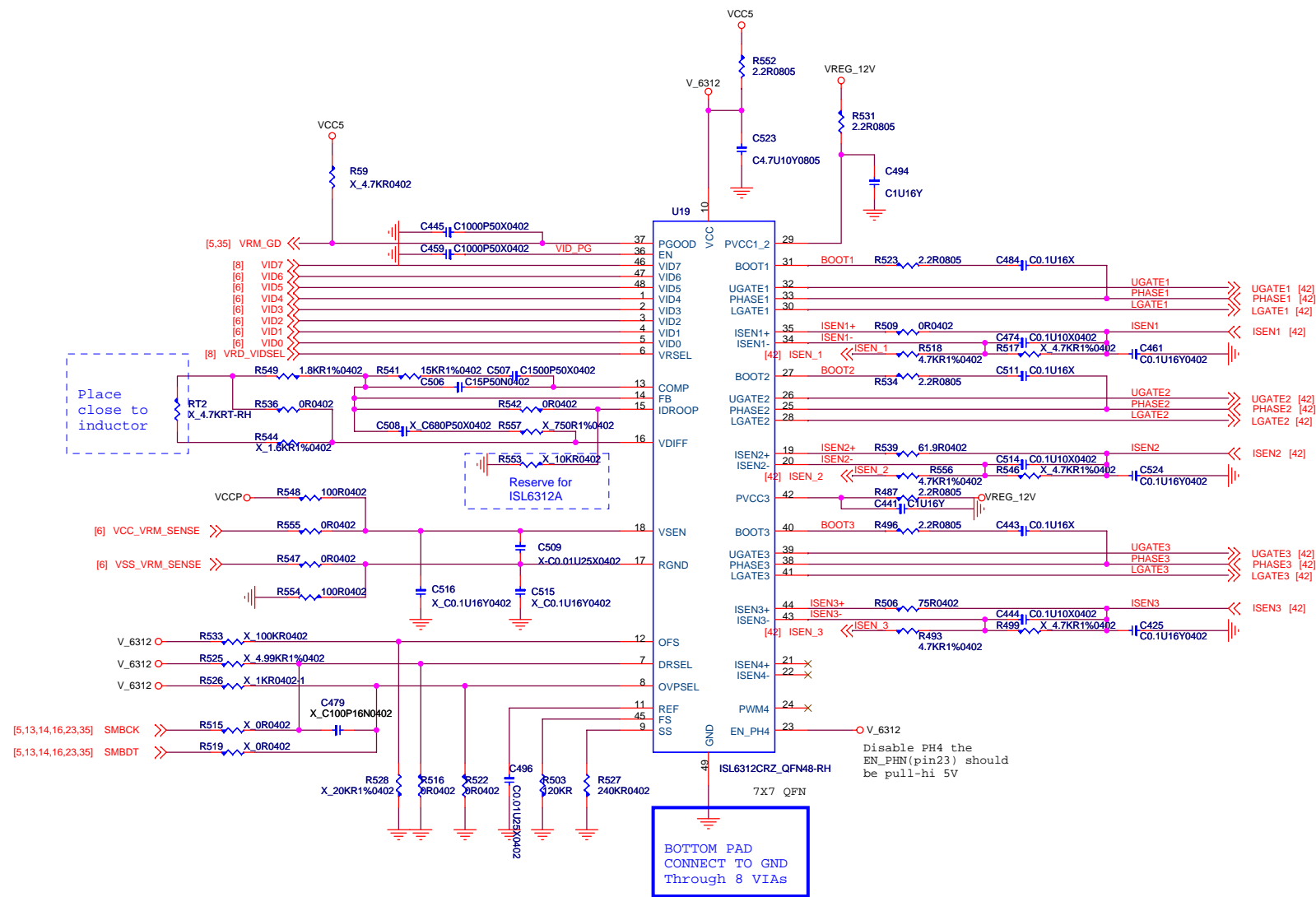


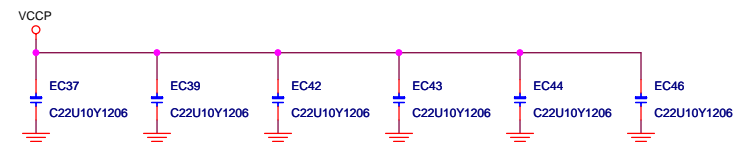
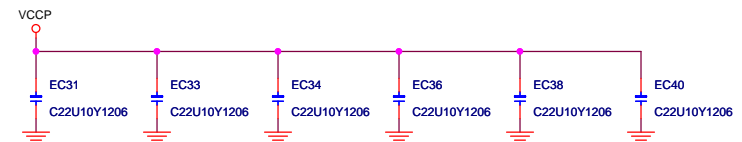
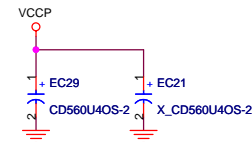
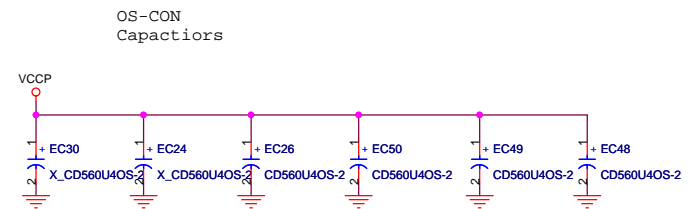
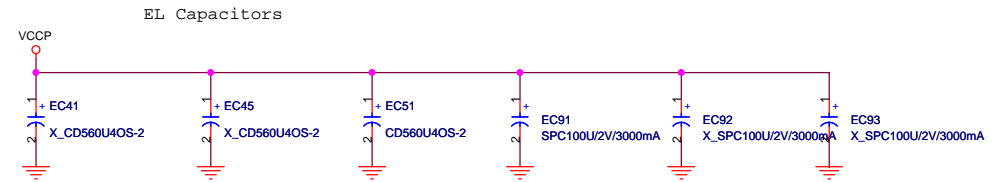
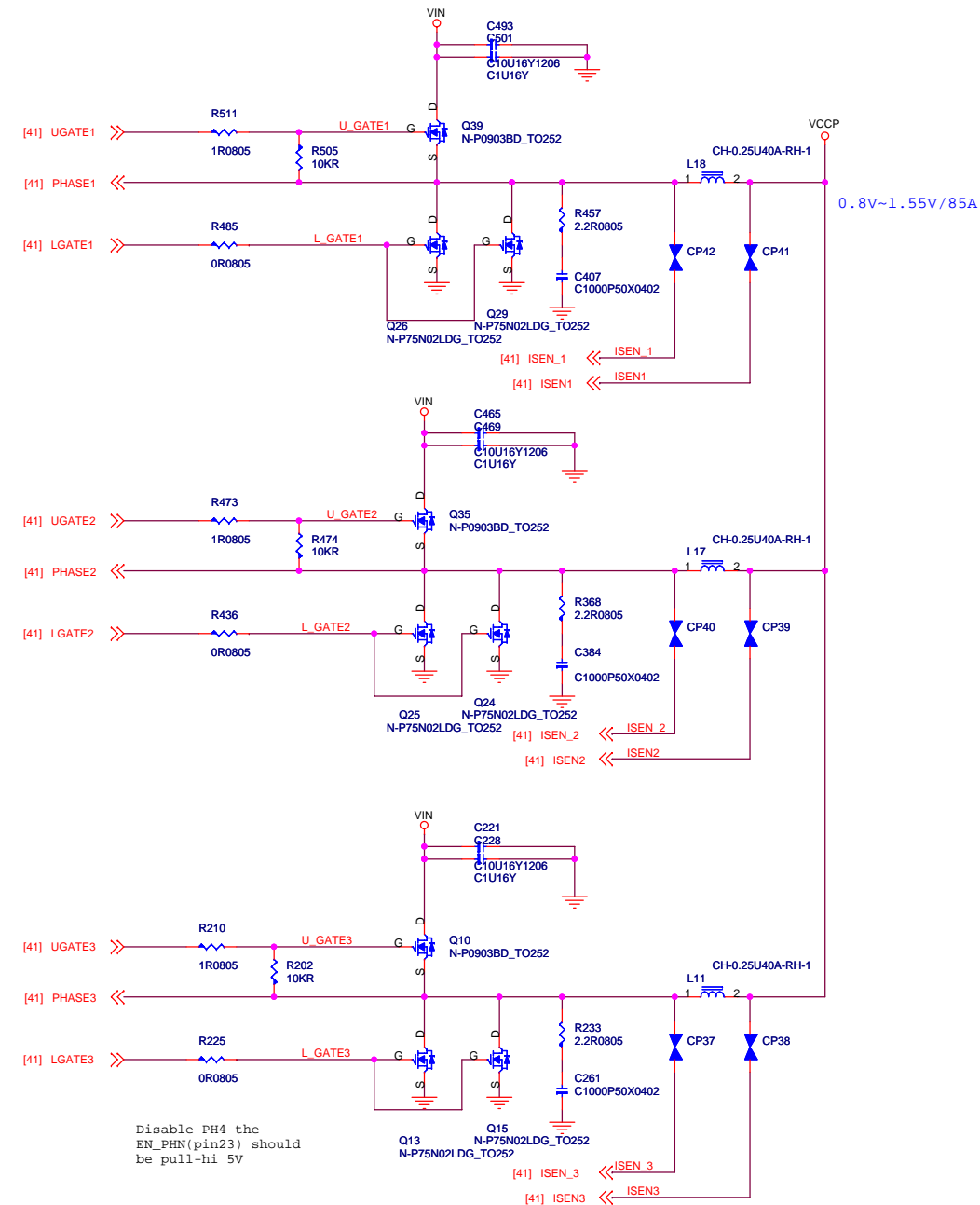
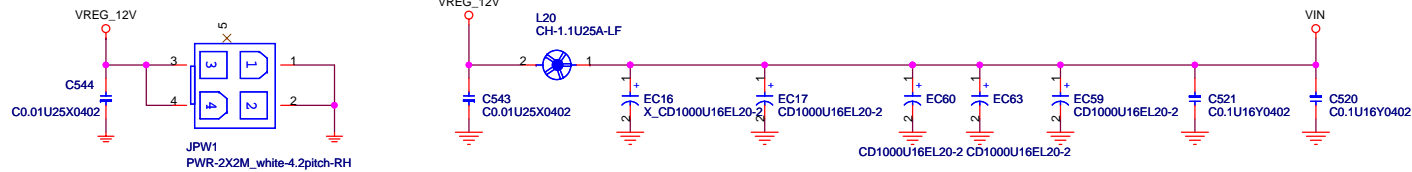


NMOS

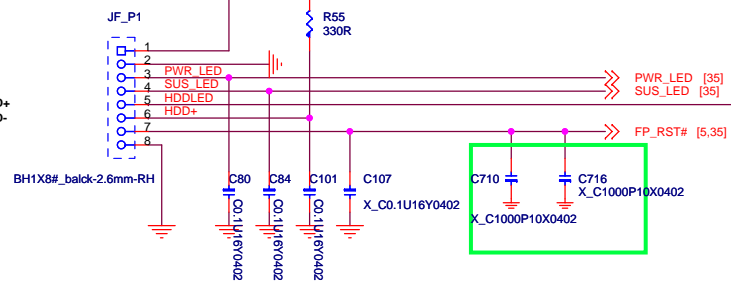
D03-0903BDB-N03
D03-50N033B-N03
D03-60N020B-O05



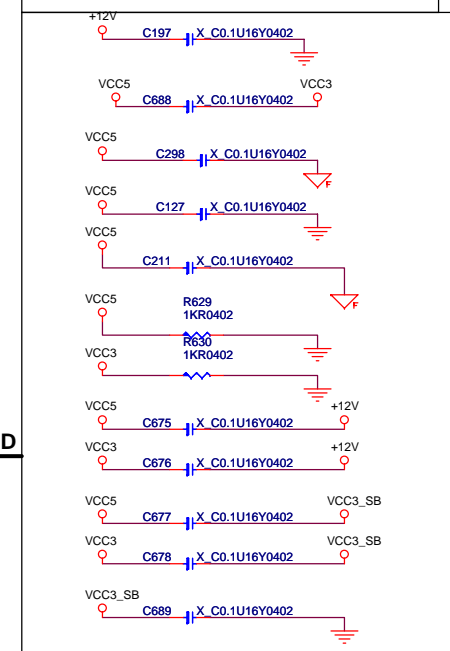
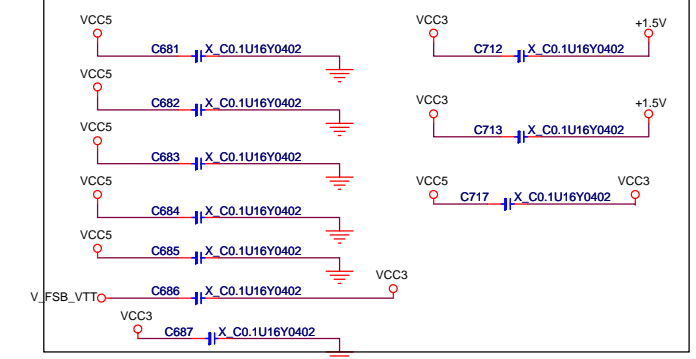
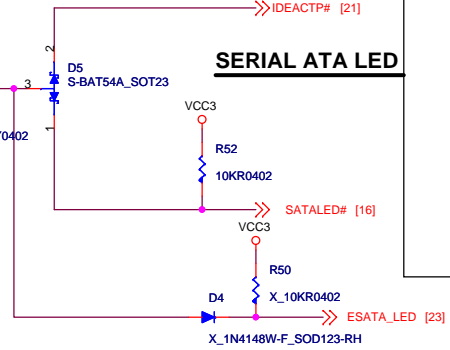


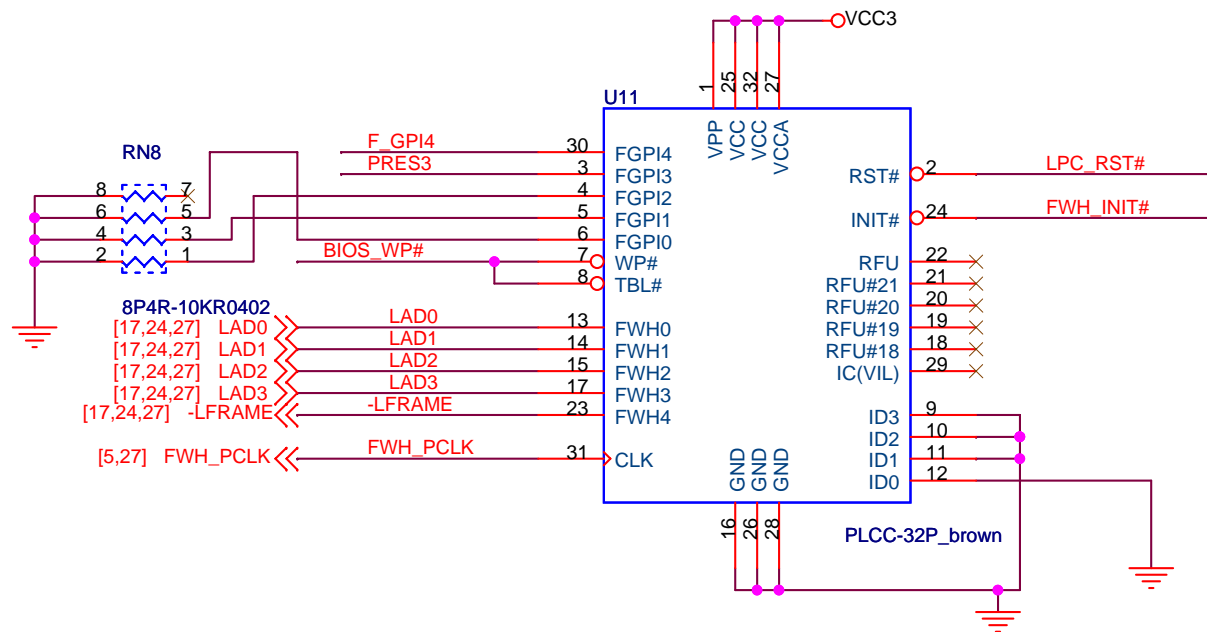


JF_P1
PIN1 PWSW-
PIN2 PWSW+
PIN3 PLED1
PIN4 PLED2
PIN5 HDD LED+
PIN6 HDD LED-
PIN7 RESET#
PIN8 GND

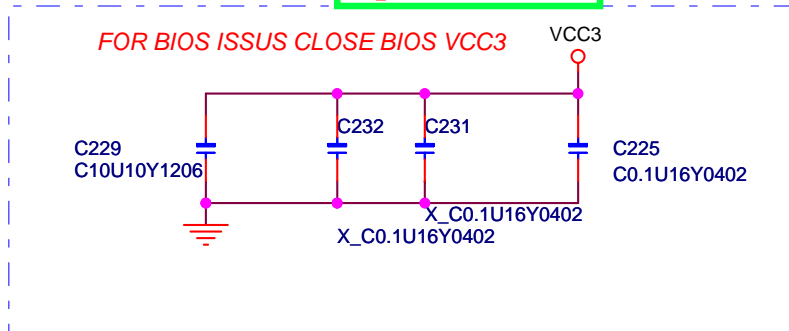
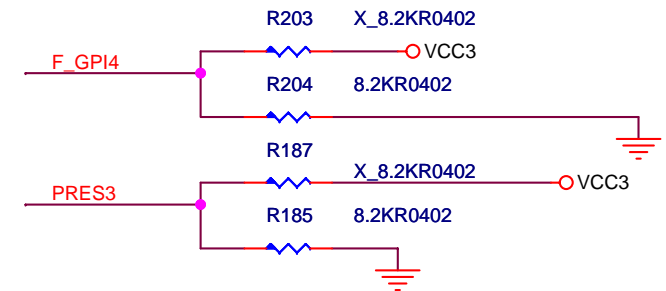
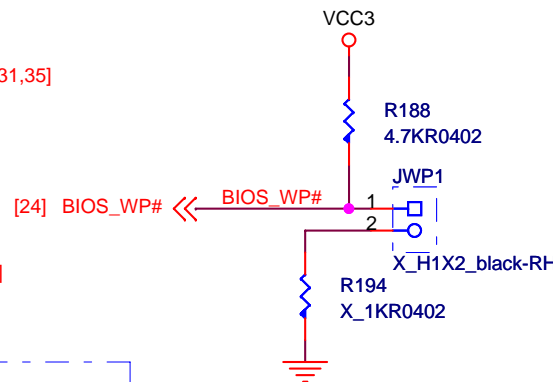
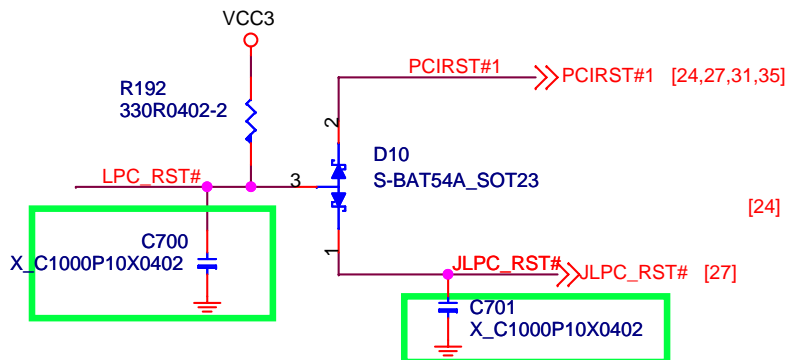
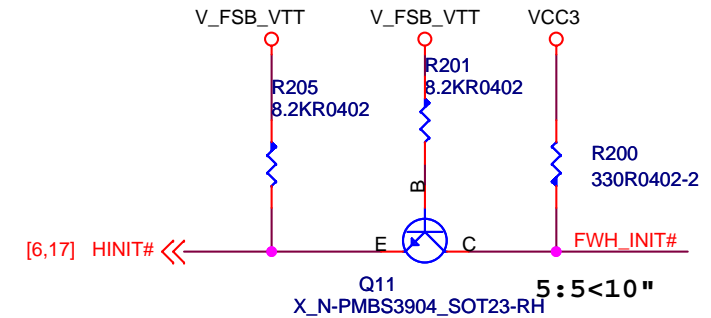


SERIAL ATA LED





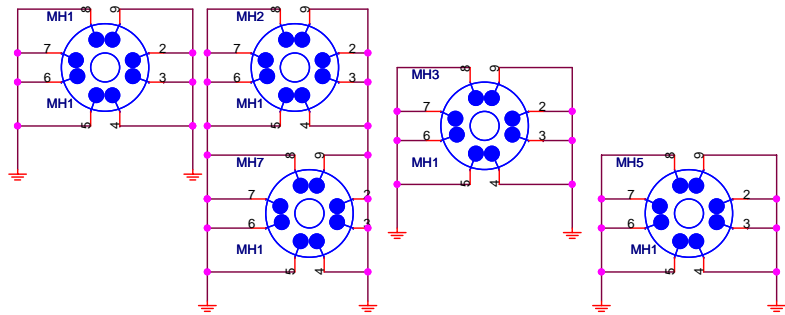
FWH INIT Signal Voltage Translation



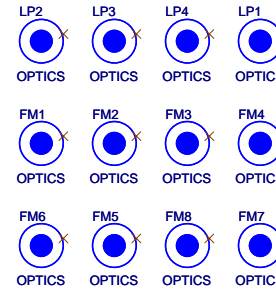
OPEN : Un_Protected
CLOSE : Protected

Micro Star Restricted Secret		
Title	Winbond & FDD & LPC & BIOS	Rev 100
Document Number	MS-7318-101-060918A	
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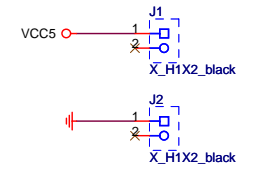
Mounting Holes



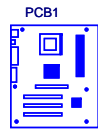
Optical Fiducial Marks



Simulation



MANUAL PART



2N7002
Top View

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Title	MISC	Rev 100
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